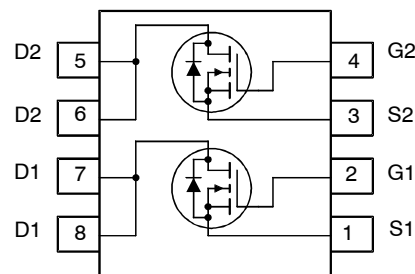


### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$  and fast switching speed.

### Features

- $V_{DS(V)} = 30V$
- $I_D = 7.5A$  ( $V_{GS} = 10V$ )
- $R_{DS(ON)} < 18m\Omega$  ( $V_{GS}=10V$ )
- $R_{DS(ON)} < 21 m\Omega$  ( $V_{GS}=4.5V$ )
- High Performance Trench Technology for Extremely Low  $r_{DS(on)}$
- Low Gate Charge
- High Power and Current Handling Capability



### Applications

- DC/DC Converters

### MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ C$ unless otherwise noted)

Symbol	Parameter	Ratings	Unit	
$V_{DSS}$	Drain to Source Voltage	30	V	
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V	
$I_D$	Drain Current	Continuous ( $T_A = 25^\circ C$ , $V_{GS} = 10 V$ , $R_{\theta JA} = 50^\circ C/W$ )	7.5	A
		Continuous ( $T_A = 25^\circ C$ , $V_{GS} = 4.5 V$ , $R_{\theta JA} = 50^\circ C/W$ )	6.9	A
		Pulsed	49	A
$E_{AS}$	Single Pulse Avalanche Energy (Note 1)	57	mJ	
$P_D$	Power Dissipation	1.6	W	
	Derate above $25^\circ C$	13	mW/ $^\circ C$	
$T_J, T_{STG}$	Operating and Storage Temperature	-55 to 150	$^\circ C$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Starting  $T_J = 25^\circ C$ ,  $L = 1 mH$ ,  $I_{AS} = 7.5 A$ ,  $V_{DD} = 30 V$ ,  $V_{GS} = 10 V$ .

### THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2)	40	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2a)	78	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 2b)	135	$^{\circ}\text{C}/\text{W}$

2.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.
- $78^{\circ}\text{C}/\text{W}$  when mounted on a  $0.5\text{ in}^2$  pad of 2 oz copper.
  - $125^{\circ}\text{C}/\text{W}$  when mounted on a  $0.02\text{ in}^2$  pad of 2 oz copper.
  - $135^{\circ}\text{C}/\text{W}$  when mounted on a minimum pad.

### ELECTRICAL CHARACTERISTICS ( $T_J = 25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$B_{V_{DS}}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	30			V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
		$V_{DS} = 24\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 150^{\circ}\text{C}$			250	
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}$			$\pm 100$	nA
$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.2		2.5	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 7.5\ \text{A}, V_{GS} = 10\ \text{V}$		14	18	m $\Omega$
		$I_D = 6.9\ \text{A}, V_{GS} = 4.5\ \text{V}$		17	21	
		$I_D = 7.5\ \text{A}, V_{GS} = 10\ \text{V}, T_J = 150^{\circ}\text{C}$		22	29	
$C_{ISS}$	Input Capacitance	$V_{DS} = 15\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$		907	1270	pF
$C_{OSS}$	Output Capacitance			191		pF
$C_{RSS}$	Reverse Transfer Capacitance			112		pF
$R_G$	Gate Resistance	$V_{GS} = 0.5\ \text{V}, f = 1\ \text{MHz}$		1.2	4.0	$\Omega$
$Q_{g(TOT)}$	Total Gate Charge at 10 V	$V_{GS} = 0\ \text{V to } 10\ \text{V}, V_{DD} = 15\ \text{V}, I_D = 7.5\ \text{A}$		17	26	nC
$Q_{g(5)}$	Total Gate Charge at 5 V	$V_{GS} = 0\ \text{V to } 5\ \text{V}, V_{DD} = 15\ \text{V}, I_D = 7.5\ \text{A}$		9	14	nC
$Q_{gs}$	Gate to Source Gate Charge	$V_{DD} = 15\ \text{V}, I_D = 7.5\ \text{A}$		2.3		nC
$Q_{gs2}$	Gate Charge Threshold to Plateau			1.5		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			3.3		nC
$t_{ON}$	Turn-On Time	$V_{DD} = 15\ \text{V}, I_D = 7.5\ \text{A}, V_{GS} = 10\ \text{V}, R_{GS} = 16\ \Omega$		44	66	ns
$t_{d(ON)}$	Turn-On Delay Time			7	10.5	ns
$t_r$	Rise Time			37	55.5	ns
$t_{d(OFF)}$	Turn-Off Delay Time			48	72	ns
$t_f$	Fall Time			24	36	ns
$t_{OFF}$	Turn-Off Time			72	108	ns
$V_{SD}$	Source to Drain Diode Voltage	$I_{SD} = 7.5\ \text{A}$			1.25	V
		$I_{SD} = 2.1\ \text{A}$			1.0	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 7.5\ \text{A}, dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$		19	25	ns
$Q_{RR}$	Reverse Recovered Charge	$I_{SD} = 7.5\ \text{A}, dI_{SD}/dt = 100\ \text{A}/\mu\text{s}$		10	13	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS  
( $T_J = 25^\circ\text{C}$  unless otherwise noted)

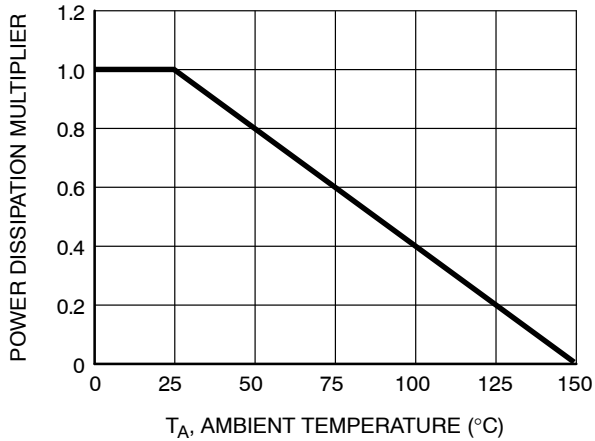


Figure 1. Normalized Power Dissipation vs. Ambient Temperature

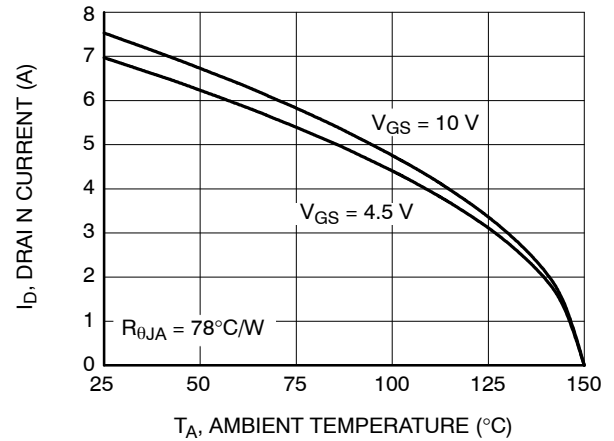


Figure 2. Maximum Continuous Drain Current vs. Ambient Temperature

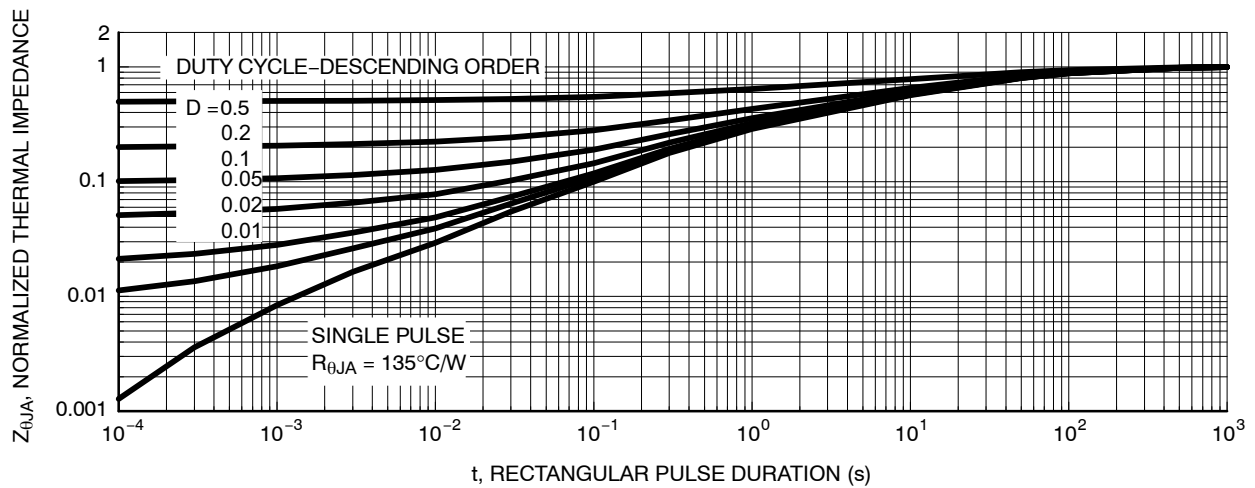


Figure 3. Normalized Maximum Transient Thermal Impedance

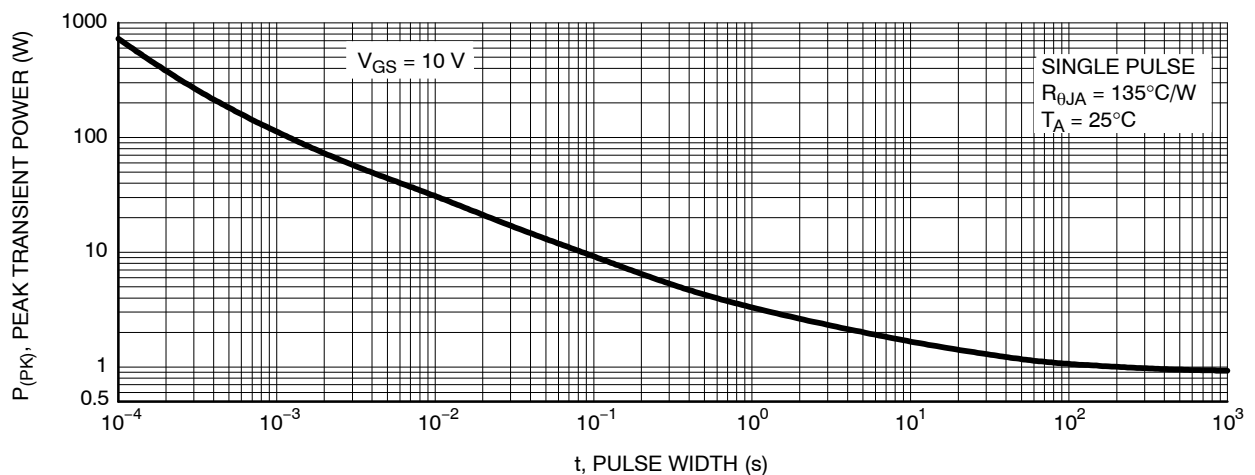
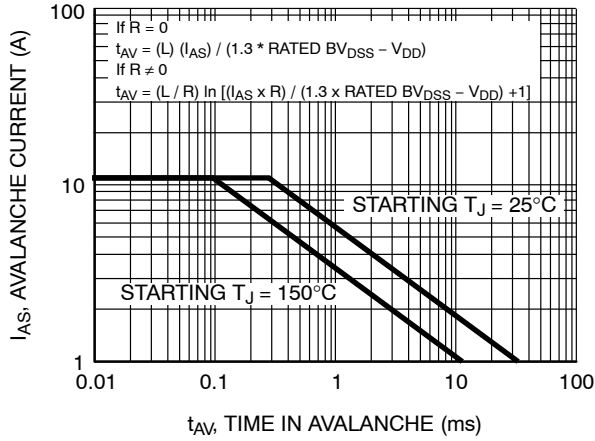
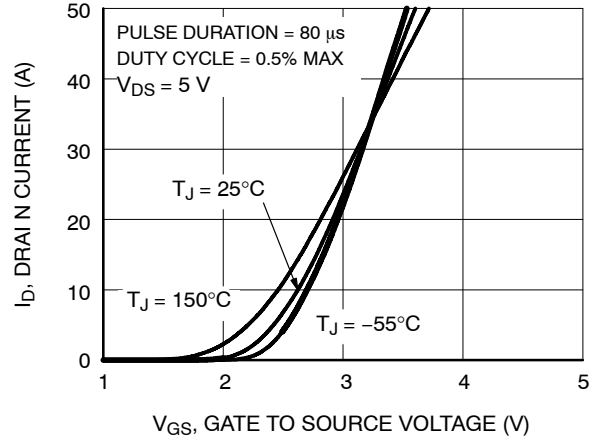


Figure 4. Single Pulse Maximum Power Dissipation

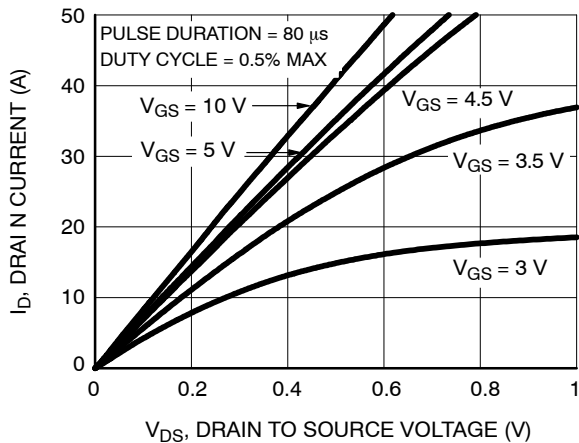
**TYPICAL CHARACTERISTICS**  
( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)



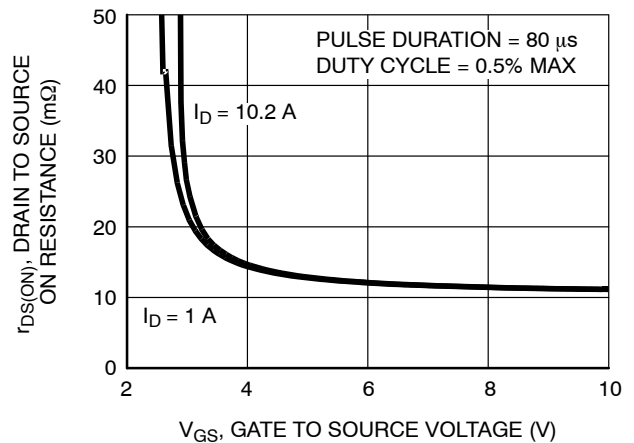
**Figure 5. Unclamped Inductive Switching Capability**



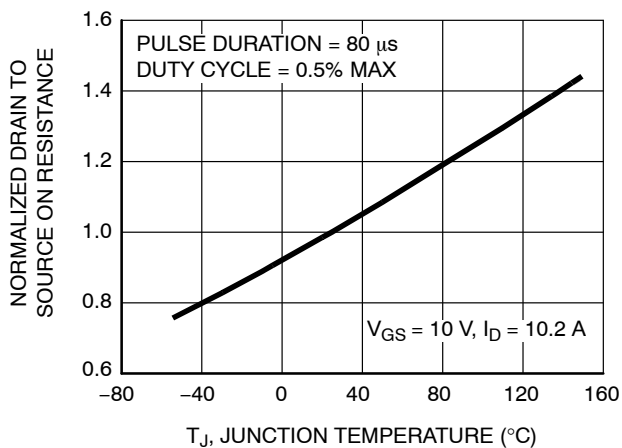
**Figure 6. Transfer Characteristics**



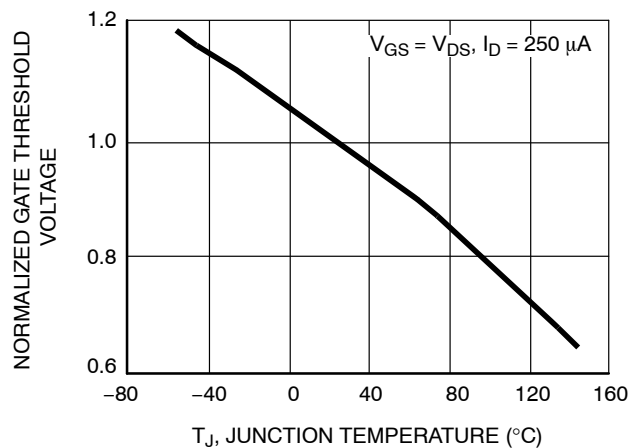
**Figure 7. Saturation Characteristics**



**Figure 8. Drain to Source On Resistance vs. Gate Voltage and Drain Current**

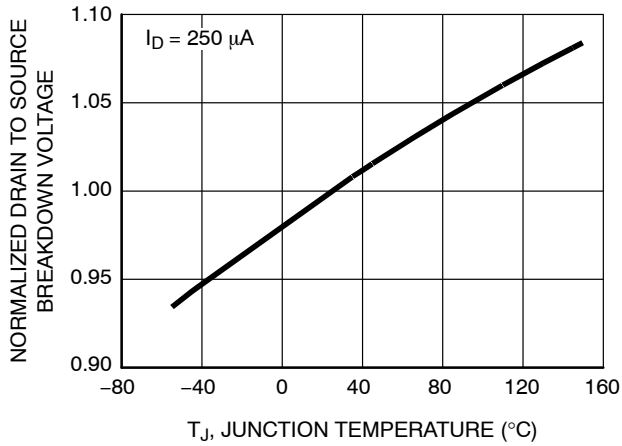


**Figure 9. Normalized Drain to Source On Resistance vs. Junction Temperature**

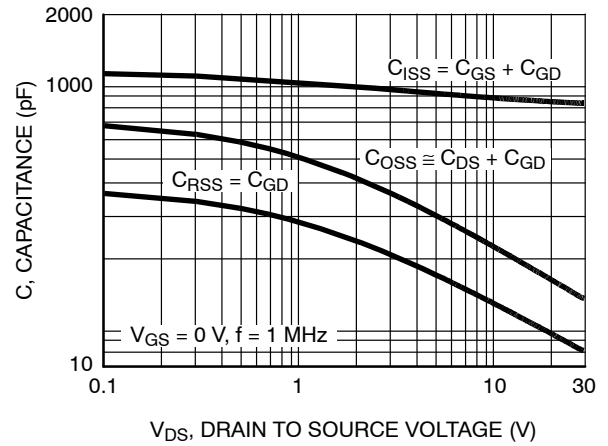


**Figure 10. Normalized Gate Threshold Voltage vs. Junction Temperature**

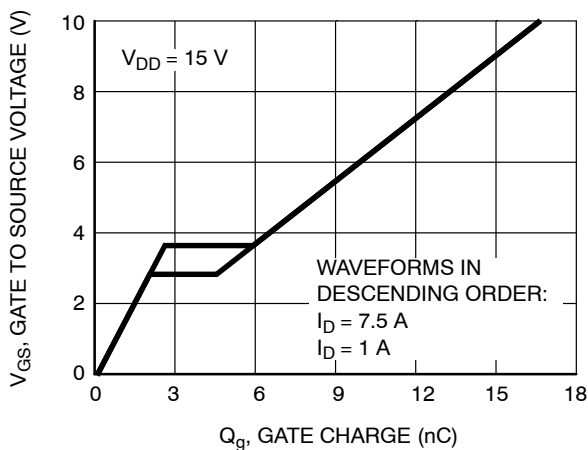
**TYPICAL CHARACTERISTICS**  
( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)



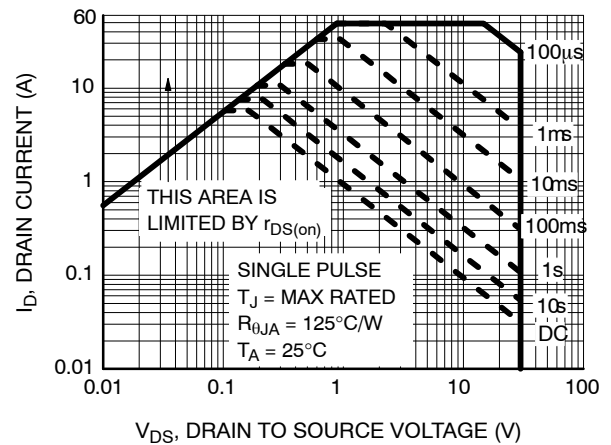
**Figure 11. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature**



**Figure 12. Capacitance vs. Drain to Source Voltage**



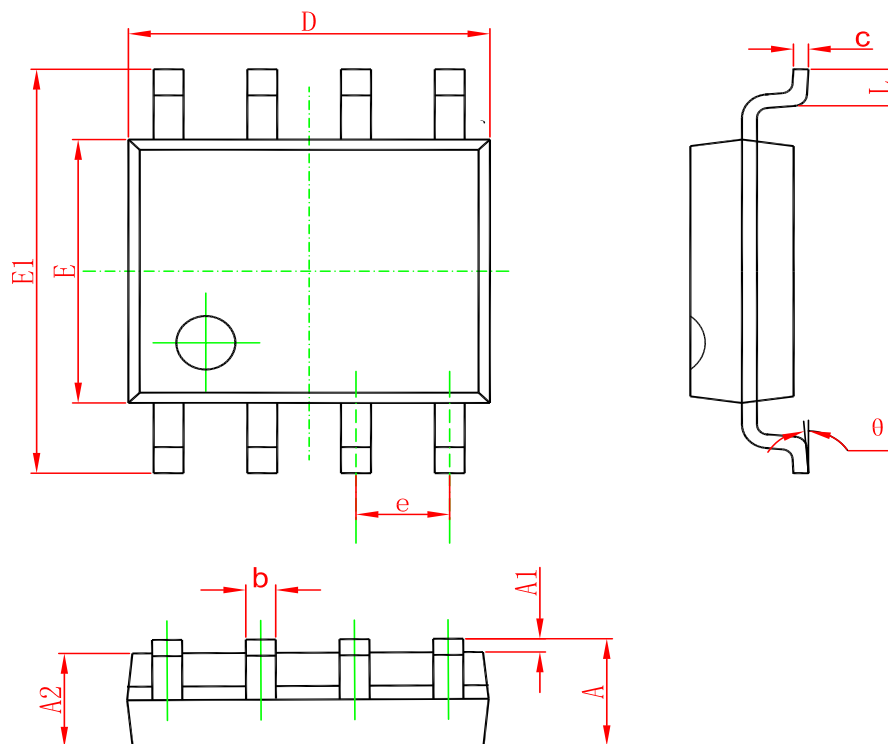
**Figure 13. Gate Charge Waveforms for Constant Gate Currents**



**Figure 14. Forward Bias Safe Operating Area**

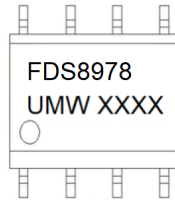
PACKAGE OUTLINE DIMENSIONS

SOP-8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

## Marking



## Ordering information

Order code	Package	Baseqty	Deliverymode
UMW FDS8978	SOP-8	3000	Tape and reel