UMW FDD7030BL

30V N-Channel MOSFET

1.Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $R_{DS(ON)}$, fast switching speed and extremely low $R_{DS(ON)}$ in a small package.

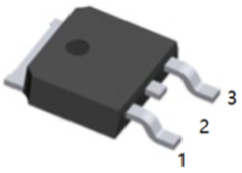
2.Features

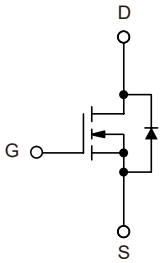
- $V_{DS\ (V)}$=30V
- I_D=56A
- $R_{DS(ON)}$<9.5mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<13mΩ(V_{GS}=4.5V)
- Low gate charge
- Fast Switching

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view





4.Absolute Maximum Ratings T_A= 25°C

Parameter			Symbol	Rating	Units
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	±20	
Continuous Drain Current	@T_C=25°C	(Note 3)	I_D	56	A
	@T_A=25°C	(Note 1a)		14	
	Pulsed	(Note 1a)		100	
Power Dissipation	@T_C=25°C	(Note 3)	P_D	60	W
	@T_A=25°C	(Note 1a)		2.8	
	@T_A=25°C	(Note 1b)		1.3	
Storage Junction Temperature Range			T_J, T_{STG}	-55 to 175	°C

5.Thermal Characteristics

Parameter		Symbol	Rating	Units
Thermal Resistance, Junction-to-Case	(Note 1)	$R_{\theta JC}$	2.5	°C/W
Thermal Resistance, Junction-to-Ambient	(Note 1a)	$R_{\theta JA}$	45	°C/W
Thermal Resistance, Junction-to-Ambient	(Note 1b)	$R_{\theta JA}$	96	°C/W

6.Electrical Characteristic (T_A=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Avalanche Energy	E_{AS}	Single Pulse, V_{DD}=15V, I_D=14A			174	mJ
Drain-Source Avalanche Current	I_{AS}				14	A
Drain–Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250μA	30			V
Breakdown Voltage Temperature Coefficient	$\frac{\Delta BV_{DSS}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		26		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=24V, V_{GS}=0V			1	μA
Gate–Body Leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1	1.8	3	V
Gate Threshold Voltage Temperature Coefficient	$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	I_D=250μA Referenced to 25°C		-5		mV/°C
Static Drain–Source On–Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=14A		7.5	9.5	mΩ
		V_{GS}=4.5V, I_D=12A		9.6	13	mΩ
On–State Drain Current	$I_{D(ON)}$	V_{GS}=10V, V_{DS}=5V	50			A
Forward Transconductance	g_{FS}	V_{DS}=10V, I_D=14A		56		S
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, f=1MHz		1425		pF
Output Capacitance	C_{oss}			350		pF
Reverse Transfer Capacitance	C_{rss}			150		pF
Gate Resistance	R_g	V_{OSC}=15mV, f=1MHz		1.3		ns
Turn-On DelayTime	$t_{D(on)}$	V_{DD}=15V, I_D=1A V_{GS}=10V, R_{GEN}=6Ω		11	20	ns
Turn-On Rise Time	t_r			9	18	ns
Turn-Off DelayTime	$t_{D(off)}$			31	50	ns
Turn-Off Fall Time	t_f	V_{DS}=15V, I_D=14A V_{GS}=5V		13	23	ns
Total Gate Charge	Q_g			14	20	nC
Gate–Source Charge	Q_{gs}			4		nC
Gate–Drain Charge	Q_{gd}			5		nC

Maximum Continuous Drain–Source Diode Forward Current	I_S				2.3	A
Drain–Source Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_S=2.3A (Note 2)		0.74	1.2	V
Diode Reverse Recovery Time	t_{rr}	I_F=14A, dIF/dt=100A/μs		23		ns
Diode Reverse Recovery Charge	Q_{rr}			11		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.

$R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) $R_{\theta JA}$=45°C/W when mounted on a 1in ^{2} pad of 2oz copper.



b) $R_{\theta JA}$= 96°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

3. Maximum current is calculated as: $\sqrt{\frac{P_D}{R_{DS(ON)}}}$

where P_D is maximum power dissipation at T_C=25°C and $R_{DS(ON)}$ is at $T_{J(max)}$ and V_{GS}=10V. Package current limitation is 21A.

7.1Typical characteristic

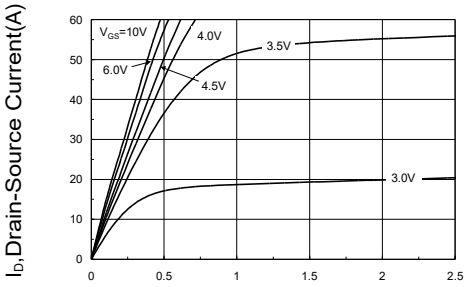


Figure 1: On-Region Characteristics

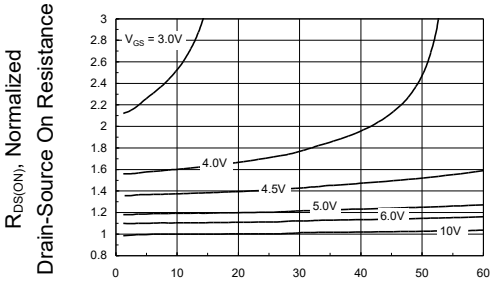


Figure 2: On-Resistance Variation with Drain Current and Gate Voltage

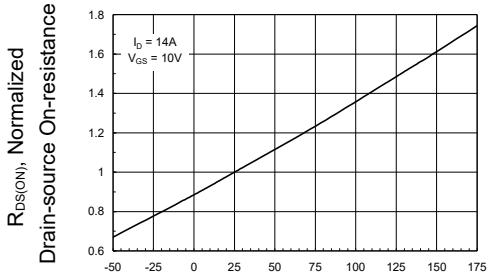


Figure 3: On-Resistance Variation with Temperature

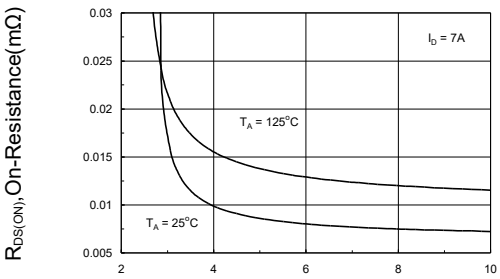


Figure 4: On-Resistance Variation with Gate-to-Source Voltage

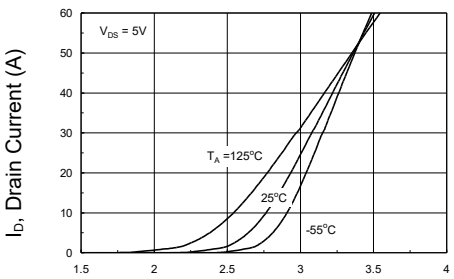


Figure 5: Transfer Characteristics

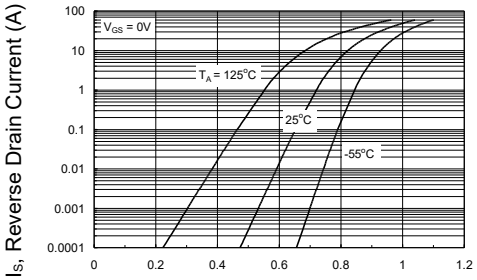
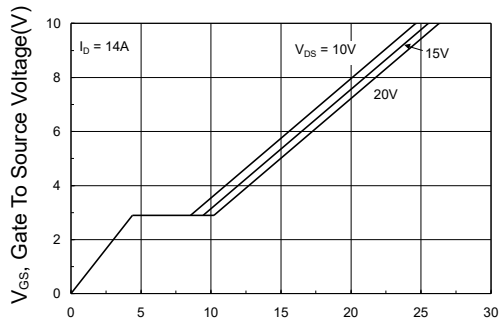


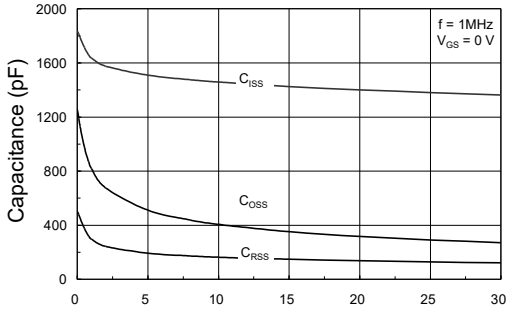
Figure 6: . Body Diode Forward Voltage Variation with Source Currentand Temperature

7.2Typical characteristic



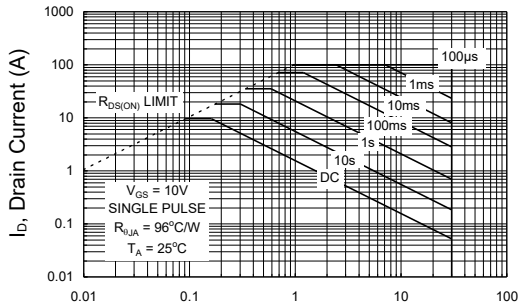
Q_g, Gate Charge (nC)

Figure 7: Gate Charge Characteristics



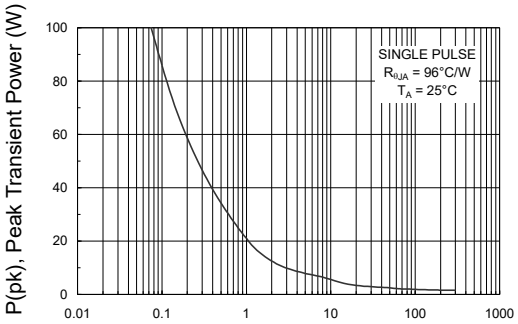
$V_{DS,}$ Drain To Source Voltage (V)

Figure 8: Capacitance Characteristics



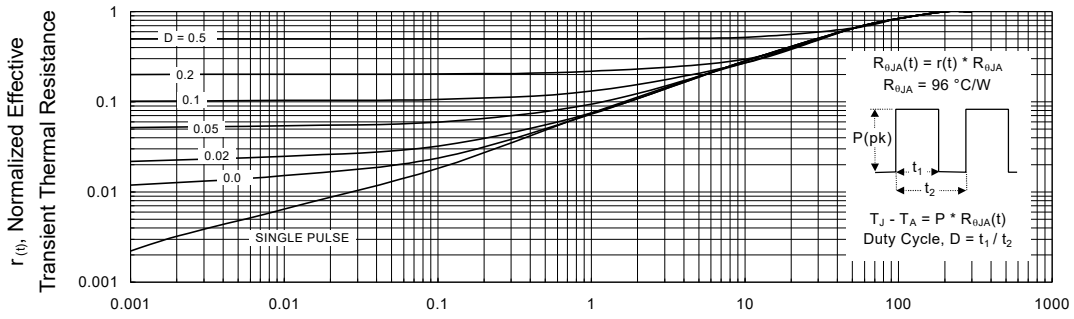
V_{DS}, Drain-source Voltage (V)

Figure 9: Maximum Safe Operating Area



t_1, TIME (sec)

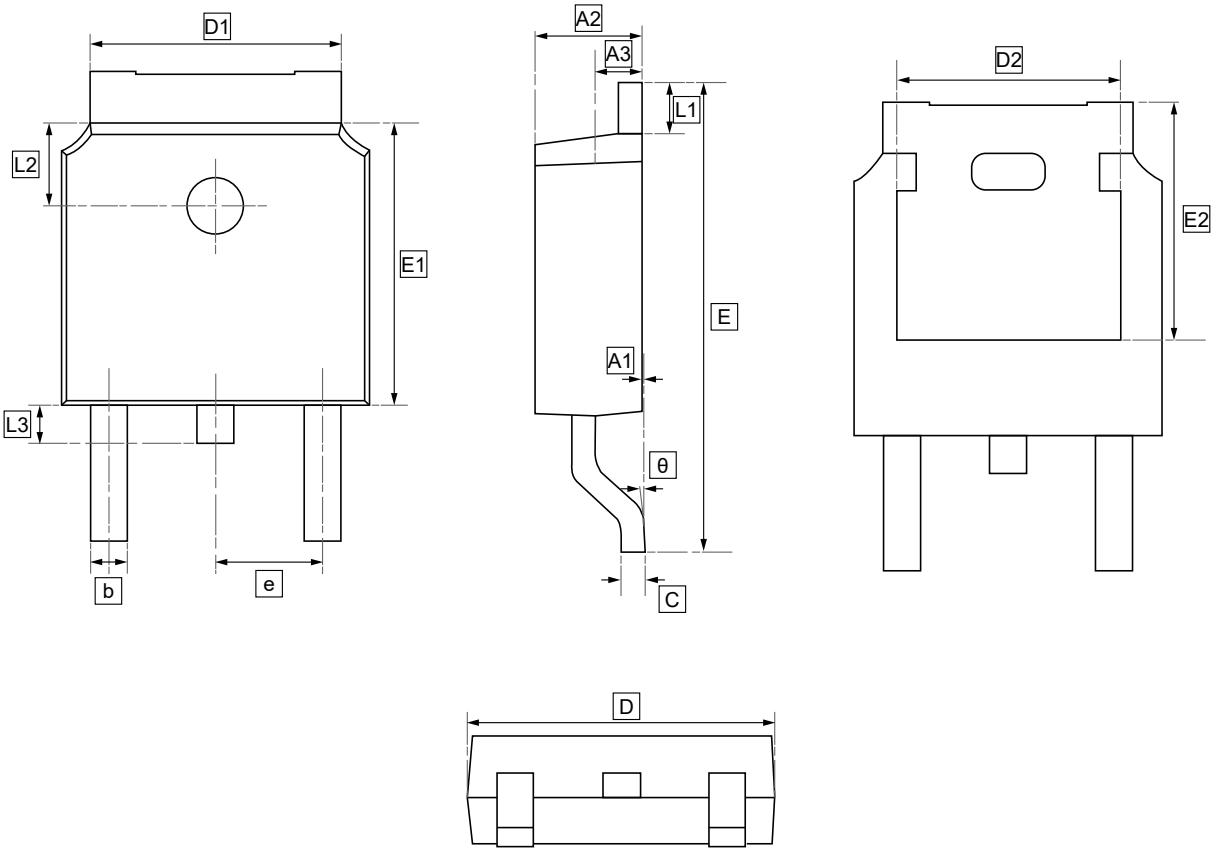
Figure 10: Single Pulse Maximum Power Dissipation



t_1, TIME (sec)

Figure 11: Transient Thermal Response Curve

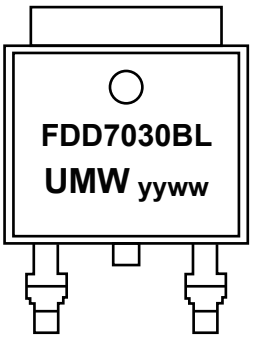
8.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDD7030BL	TO-252	2500	Tape and reel

10.Disclaimer

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