UMW FDS6681Z

-30V P-Channel MOSFET

1.Features

- $V_{DS(V)}$=-30V
- Q_g=27nC
- I_D=-18A
- $R_{DS(ON)}$<5mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<8mΩ(V_{GS}=4.5V)

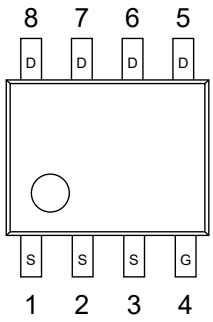
2.Applications

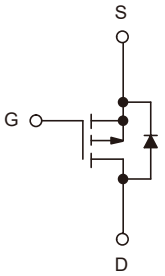
- Battery management in mobile devices
- Adapter and charger switch
- Battery switch
- Load switch

3.Pinning information

Pin	Symbol	Description
1,2,3	S	SOURCE
4	G	GATE
5,6,7,8	D	DRAIN

SOP-8





4.Maximum ratings (T_A=25°C unless otherwise noted)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous DrainCurrent (T_J = 150 °C)	T_C=25°C	I_D	-18	A
	T_C=70°C		-13	
	T_A=25°C		-11	
	T_A=70°C		-8	
Pulsed Drain Current (t=100μs)		I_{DM}	-145	
Continuous Source-Drain Diode Current	T_C=25°C	I_S	-5	
	T_A=25°C		-2.8[b,c]	

Single pulse avalanche current	L = 0.1 mH	I_{AS}	-25	A
Single pulse avalanche energy		E_{AS}	31.2	mJ
Maximum Power Dissipation	T_C=25°C	I_P	5.6	W
	T_C=70°C		3.6	
	T_A=25°C		3.1[b,c]	
	T_A=70°C		2[b,c]	
Storage Temperature Range		T_J,T_{STG}	-55 to 150	°C
Soldering recommendations (peak temperature)[c]			260	°C

5.Thermal resistance rating

Parameter		Symbol	Typ	Max	Units
Maximum junction-to-ambient [b]	t ≤10s	R_{thJA}	34	40	°C/W
Maximum junction-to-case (drain)	Steady-State	R_{thJF}	18	22	°C/W

Notes:

a. Package limited

b. Surface mounted on 1" x 1" FR4 board

c. t=10 s

d. The SOP-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

f. Maximum under steady state conditions is 85 °C/W

g. T_C=25 °C

6.Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS}=0V, I_D=-250μA	-30			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D=-10mA		-17		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I_D=-250μA		5.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	-1		-2.2	V
Gate-Source Leakage	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-30V, V_{GS}=0V			-1	μA
		V_{DS}=-30V, V_{GS}=0V, T_J=70°C			-15	
On-State Drain Current[a]	$I_{D(ON)}$	V_{DS}≥-10V, V_{GS}=-10V	-40			A
Drain-Source On-State Resistance[a]	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-15A		5		mΩ
		V_{GS}=-4.5V, I_D=-10A		8		
Forward Transconductance[a]	g_{FS}	V_{DS}=-15V, I_D=-15A		81		S
Dynamic [b]						
Input Capacitance	C_{iss}	V_{DS}=-15V, V_{GS}=0V, f=1MHz		3490		pF
Output Capacitanc	C_{oss}			1420		
Reverse Transfer Capacitance	C_{rss}			70		
Total Gate Charge	Q_g	V_{DS}=-15V,V_{GS}=-10V		56	84	nC
		I_D=-10A		27	41	
Gate Source Charge	Q_{gs}	V_{DS}=-15V, V_{GS}=-4.5V		9.4		
Gate Drain Charge	Q_{gd}	I_D=-10A		8.2		
Gate Resistance	R_g	f=1MHz	1.5	3.5	6	Ω
Turn-On DelayTime	$t_{D(on)}$	V_{DD} =-15V, R_L=1.5Ω		15	30	ns
Rise Time	t_r	I_D≅-10A, V_{GEN}=-10V		6	12	
Turn-Off DelayTime	$t_{D(off)}$	R_g=1Ω		39	78	
Fall Time	t_f			10	20	

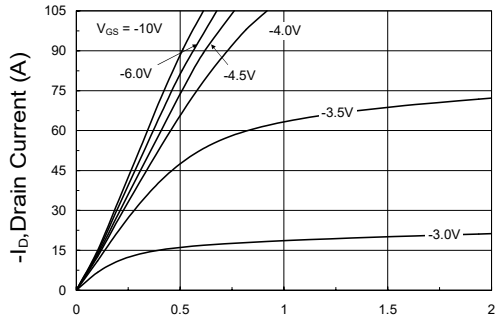
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=-15V, R_L=1.5Ω I_D≌-10V, V_{GEN}=-4.5V R_g=1Ω		34	68	ns
Rise Time	t_r			86	172	ns
Turn-Off Delay Time	$t_{D(off)}$			31	62	ns
Fall Time	t_f			22	44	ns
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C=25°C			-5	A
Pulse Diode Forward Current	I_{SM}				-150	A
Body Diode Voltage	V_{SD}	I_S=-5A, V_{GS}=0V		-0.73	-1.1	V
Body Diode Reverse Recovery Time	t_{rr}	I_F=-10A, dI/dt=100A/μs T_J=25°C		44	88	ns
Body Diode Reverse Recovery Charge	Q_{rr}			41	82	nC
Reverse Recovery Fall Time	t_a			19		ns
Reverse Recovery Rise Time	t_b			25		ns

Notes:

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

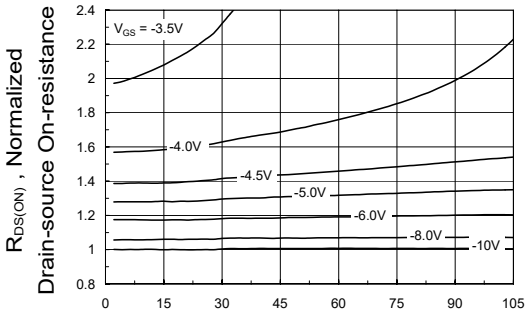
b. Guaranteed by design, not subject to production testing.

7.1Typical Characterisitics



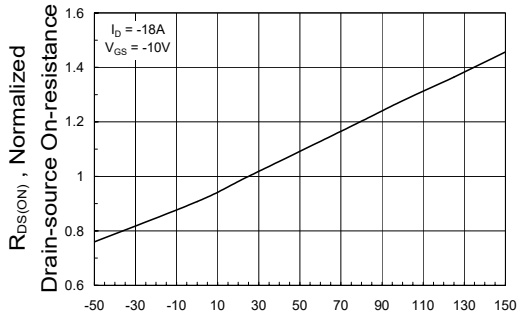
$-V_{DS}$,Drain Source Voltage (V)

Figure 1: On-Region Characteristics



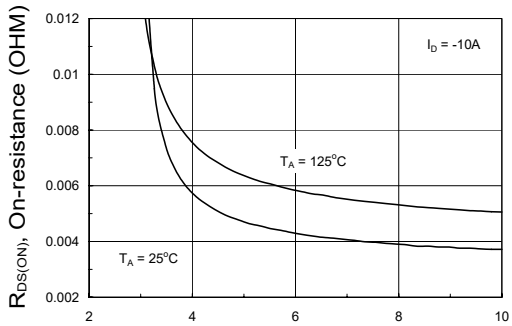
$-I_D$, Drain Current (A)

Figure 2: On-Resistance Variation with Drain Current and Gate Voltage



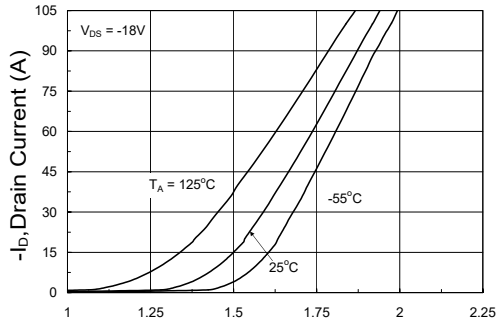
T_J,Junction Temperature (°C)

Figure 3: On-Resistance Variation with Temperature



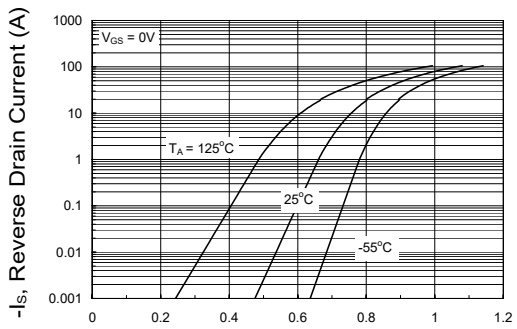
$-V_{GS}$,Gate to Source Voltage (V)

Figure 4: On-Resistance Variation with Gate-to-Source Voltage



$-V_{GS}$,Gate to Source Voltage (V)

Figure 5: Transfer Characteristics



$-V_{SD}$, Body Diode Forward Voltage (V)

Figure 6: Body Diode Forward Voltage Variation with Source Current and Temperature

7.2Typical Characterisitics

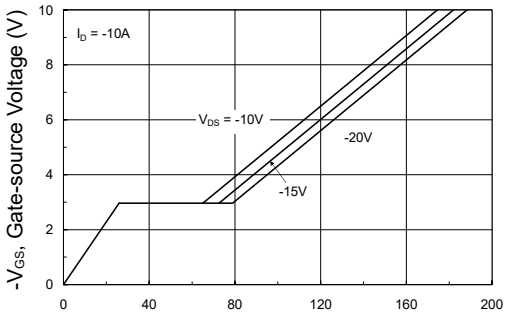


Figure 7: Gate Charge Characteristics

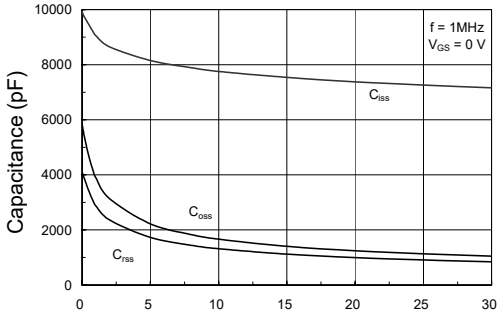


Figure 8: Capacitance Characteristics

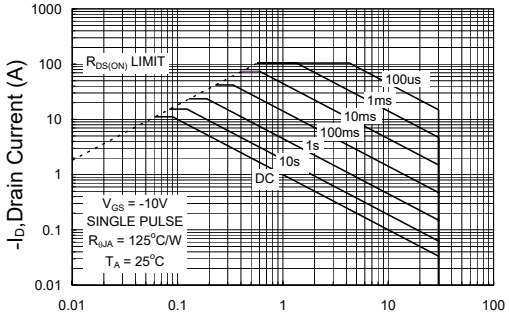


Figure 9: Maximum Safe Operating Area

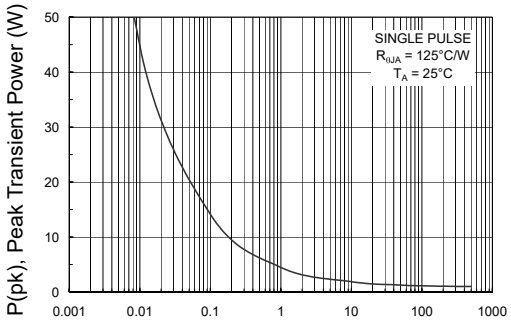


Figure 10: Single Pulse Maximum Power Dissipation

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

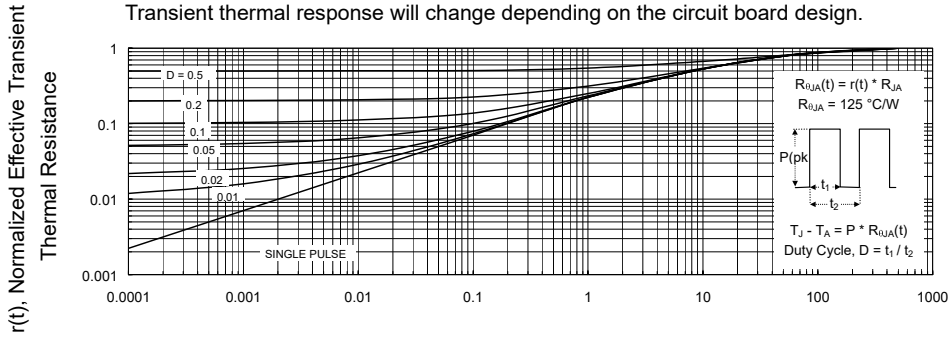
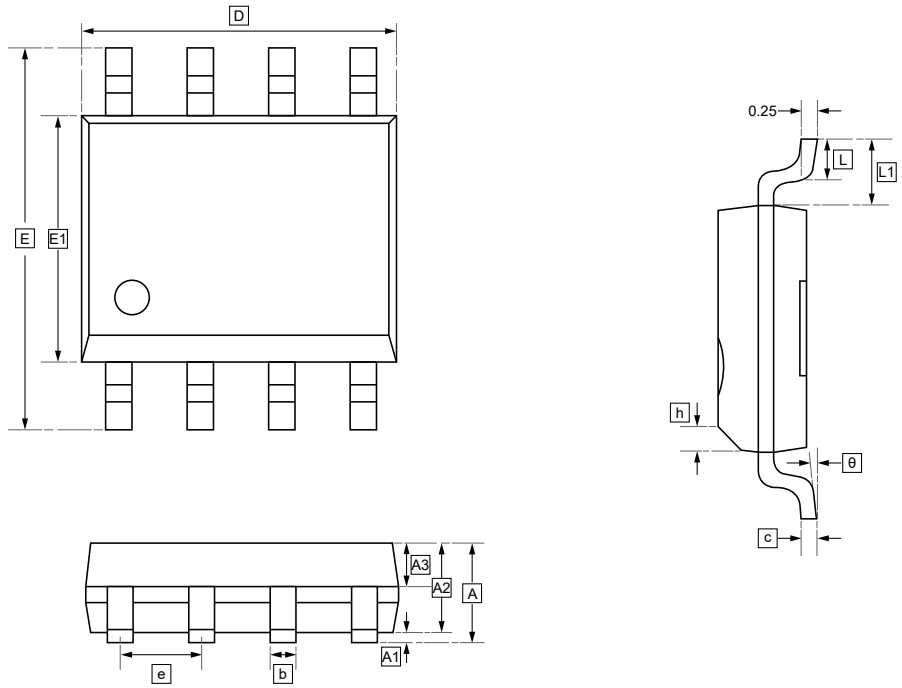


Figure 11: Transient Thermal Response Curve

8.SOP-8 Package Outline Dimensions

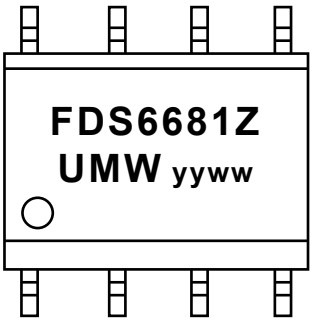


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.70	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.10	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW FDS6681Z	SOP-8	3000	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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