UMW IPD050N03LGATMA1

30V N-Channel MOSFET

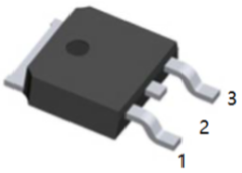
1.Features

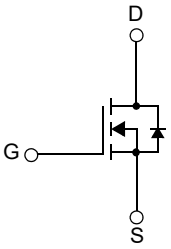
- $V_{DS\ (V)}$=30V
- I_D=50A
- $R_{DS(ON)}$<5mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<7.3mΩ(V_{GS}=4.5V)

2.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view





3.Absolute Maximum Ratings T_C= 25°C

Parameter	Symbol	Conditions	Rating	Units
Continuous drain current	I_D	V_{GS}=10V, T_C=25°C	50	A
		V_{GS}=10V, T_C=100°C	50	A
		V_{GS}=4.5V, T_C=25°C	50	A
		V_{GS}=4.5V, T_C=25°C	50	A
Pulsed drain current [2]	$I_{D,pulse}$	T_C=25°C	350	A
Avalanche energy, single pulse [3]	I_{AS}	T_C=25°C	50	A
Avalanche energy, single pulse	E_{AS}	I_D=35A, R_{GS}=25Ω	60	mJ
Reverse diode dv/dt	dv/dt	I_D=50A, V_{DS}=24V di/dt=200 A/μs, $T_{j,max}$=175°C	6	kV/μs
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25°C	68	W
Operating and storage temperature	T_J,T_{STG}		-55 to 175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

4.Electrical Characteristic (T_C=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal resistance, junction -case	R_{thJC}				2.2	K/W
SMD version, device on PCB	R_{thJA}	minimal footprint			75	K/W
		6 cm^2 cooling area [4])			50	K/W
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=1mA	30			V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1		2.2	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=30V, V_{GS}=0V, T_J=25°C		0.1	1	μA
		V_{DS}=30V, V_{GS}=0V, T_J=125°C		10	100	μA
Gate-source leakage current	I_{GSS}	V_{GS}=20V, V_{DS}=0V		10	100	nA
Drain-source on-state resistance [5])	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=30A		5.8	7.3	mΩ
		V_{GS}=10V, I_D=30A		4.2	5	mΩ
Gate resistance	R_G			1.5		Ω
Transconductance	g_{FS}	$\|V_{DS}\|>2\|I_D\|R_{DS(ON)max}$,$I_D$=30A	38	77		S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=15V, f=1MHz		2400	3200	pF
Output capacitance	C_{oss}			920	1200	pF
Reverse transfer capacitance	C_{rss}			49		pF
Turn-on delay time	$t_{D(on)}$	V_{DD}=15V, V_{GS}=10V I_D=30A, R_G=1.6Ω		6.7		ns
Rise time	t_r			13		ns
Turn-off delay time	$t_{D(off)}$			25		ns
Fall time	t_f			3.8		ns
Gate to source charge	Q_{gs}	V_{DD}=15V, I_D=30A V_{GS}=0 to 4.5V		7.4		nC
Gate charge at threshold	$Q_{g(th)}$			3.8		nC
Gate to drain charge	Q_{gd}			3.5		nC
Switching charge	Q_{SW}			7.1		nC
Gate charge total	Q_g			15	20	nC
Gate plateau voltage	$V_{plateau}$			3.1		V

Gate charge total	Q_g	V_{DD}=50V, I_D=30A, V_{GS}=0 to 10V		31		nC
Gate charge total, sync.FET	$Q_{g(sync)}$	V_{DS}=0.1V, V_{GS}=0 to 4.5V		13	17	nC
Output charge	Q_{oss}	V_{DD}=15V, V_{GS}=0V		24		nC
Diode continuous forward current	I_S	T_C=25°C			50	A
Diode pulse current	$I_{S,pulse}$				350	A
Diode forward voltage	V_{SD}	V_{GS}=0V, I_F=30A, T_J=25°C		0.86	1.1	V
Reverse recovery charge	Q_{rr}	V_R=15V, I_F=I_S, di_F/dt=400A/μs			15	nC

Notes:

6) See figure 16 for gate charge parameter definition.

5.1Typical characteristic

$P_{tot}=f(T_C)$

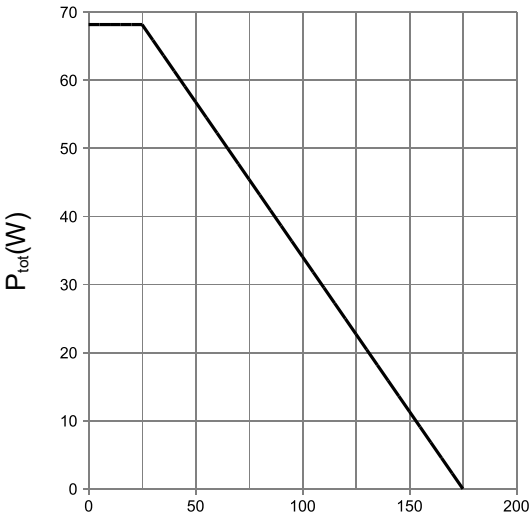


Fig 1. Power dissipation

$I_D=f(T_C)$; $V_{GS}\geq 10V$

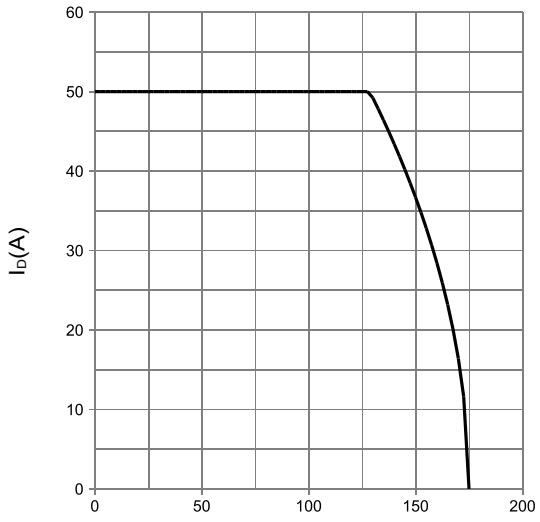


Fig 2. Drain current

ID=f(V_{DS}); T_C=25°C; D=0; parameter: t_p

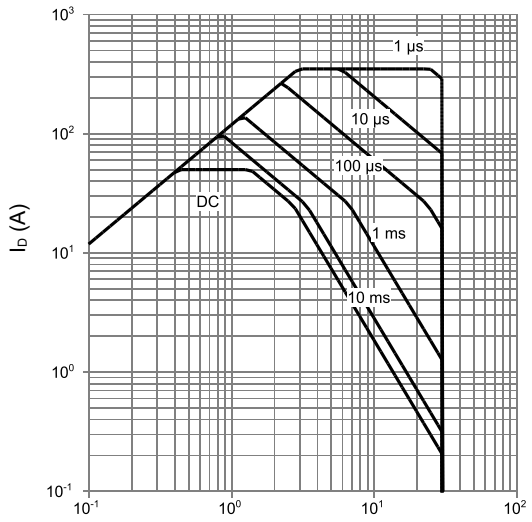


Fig 3. Safe operating area

$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

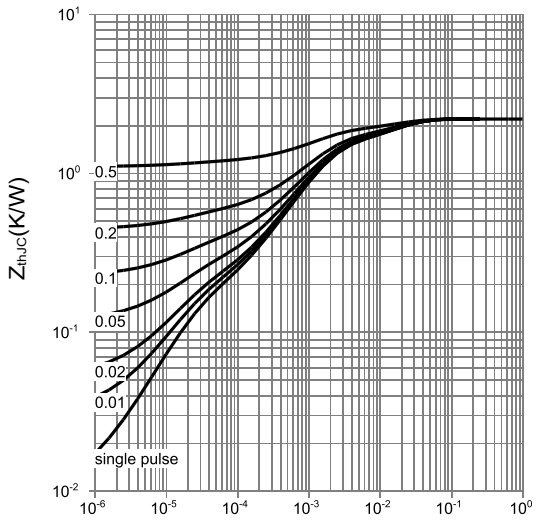


Fig 4. Max transient thermal impedance

5.2Typical characteristic

$I_D=f(V_{DS})$; T_J=25°C; parameter: V_{GS}

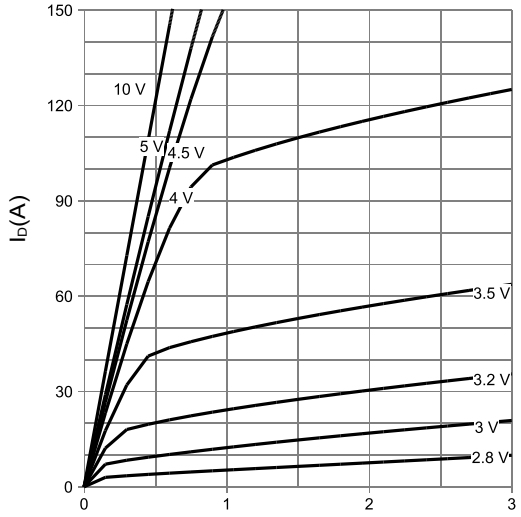


Fig 5. output characteristics

$R_{DS(ON)}=f(I_D)$; T_J=25°C; parameter: V_{GS}

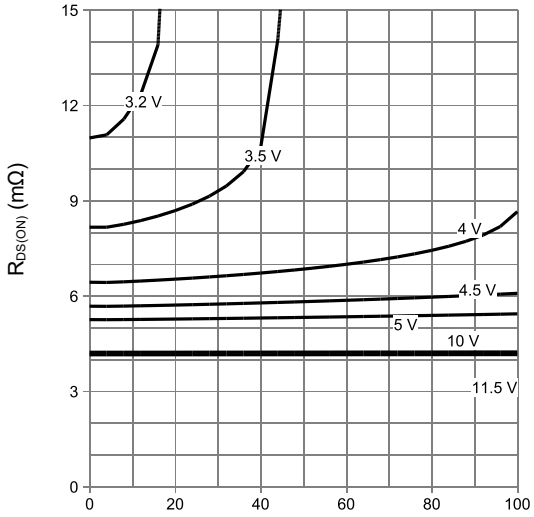


Fig 6. drain-source on resistance

ID=f(V_{GS}); |V_{DS}|>2| I_D |$R_{DS(ON)max}$; parameter: T_J

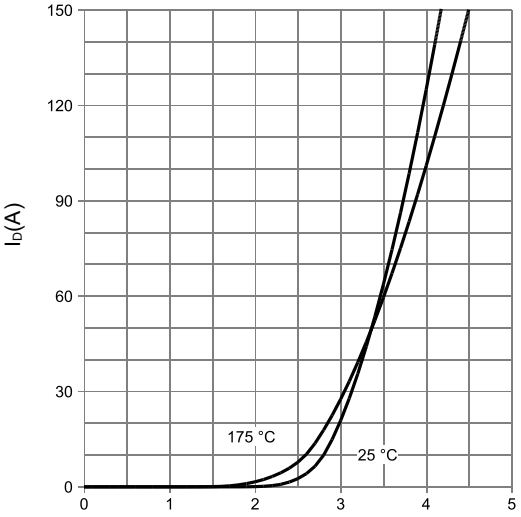


Fig 7. transfer characteristics

$g_{fs}=f(I_D)$; T_J=25°C

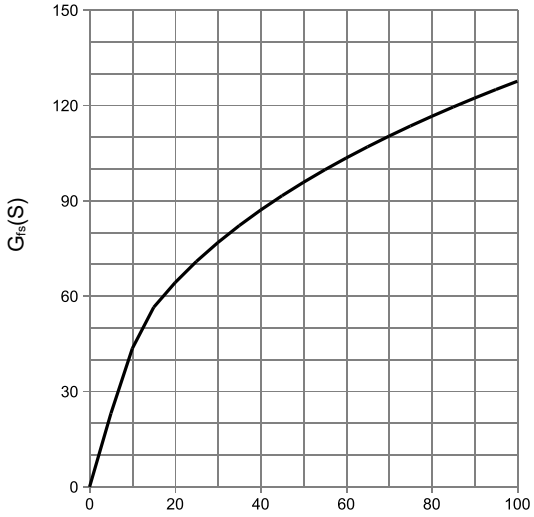


Fig 8. forward transconductance

5.3Typical characteristic

$R_{DS(ON)}=f(T_J)$; I_D=30A; V_{GS}=10V

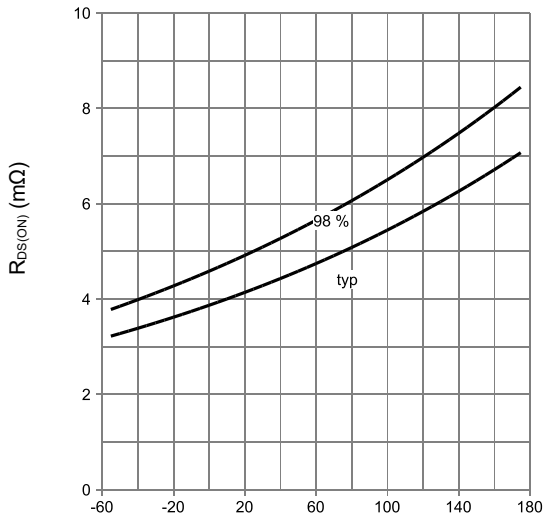


Fig 9. Drain-source on-state resistance

$V_{GS(th)}=f(T_J)$;$V_{GS}=V_{DS}$; I_D=250μA

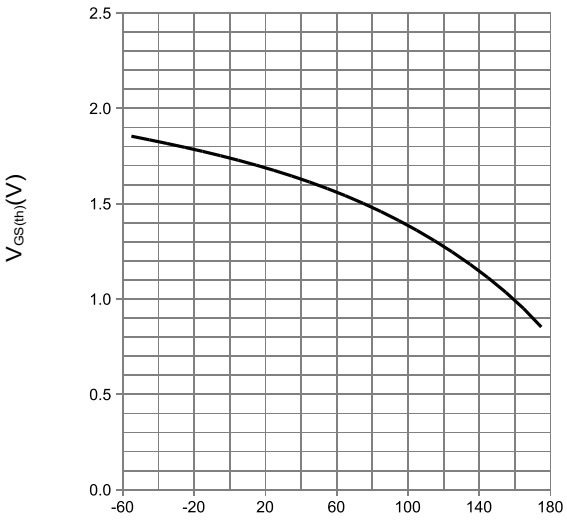


Fig 10. Gate threshold voltage

C=f(V_{DS}); V_{GS}=0V; f=1MHZ

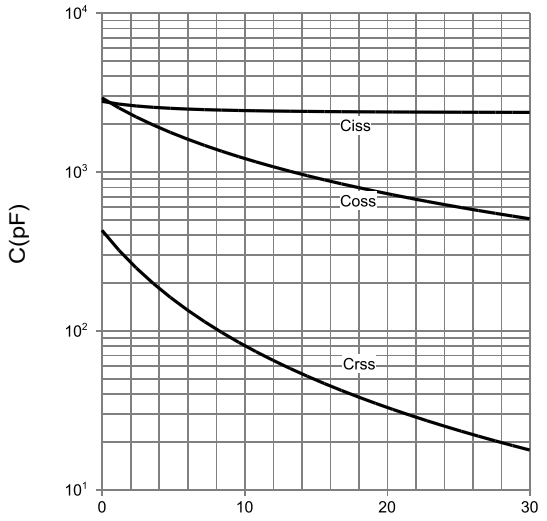


Fig 11. capacitances

I_F=f(V_{SD}); parameter: T_J

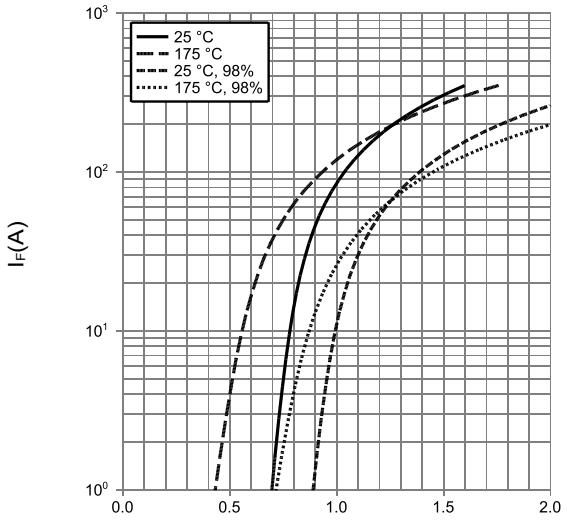


Fig 12. Forward characteristics of reverse diode

5.4Typical characteristic

$I_{AS}=f(t_{AV})$; $R_{GS}=25\Omega$; parameter: $T_{j(start)}$

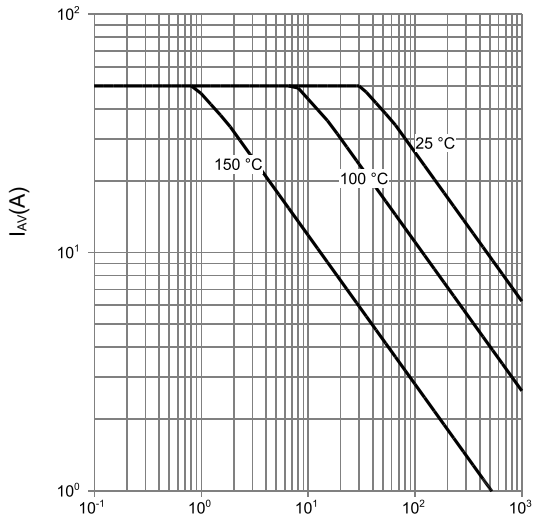


Fig 13. Avalanche characteristics

$V_{GS}=f(Q_{gate})$; $I_D=30A$pulsed; parameter: V_{DD}

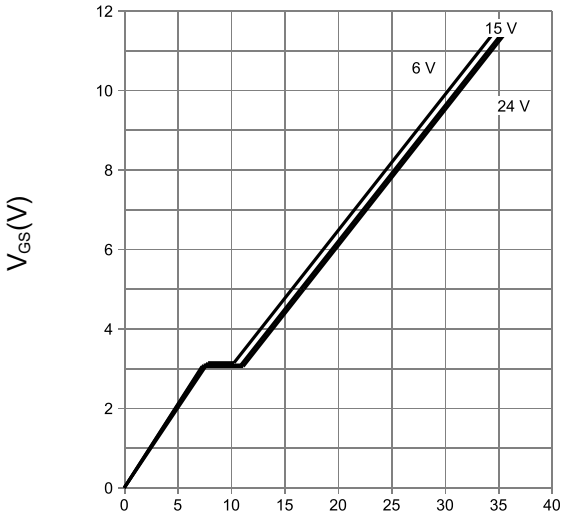


Fig 14. gate charge

$V_{BR(DSS)}=f(T_J)$; I_D=1m A

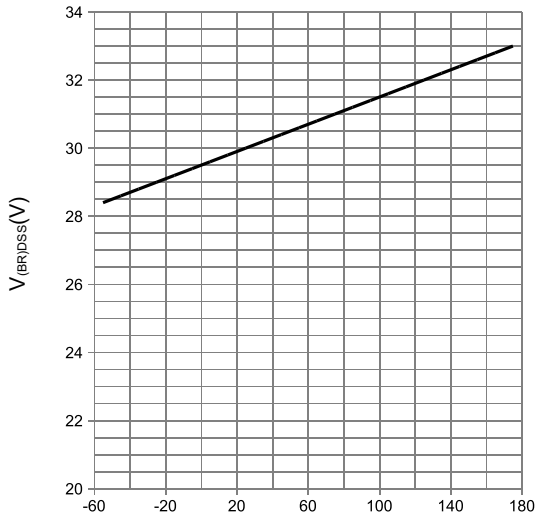


Fig 15. drai source breakdown voltage

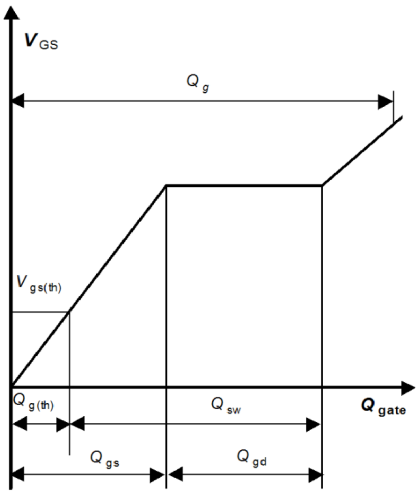
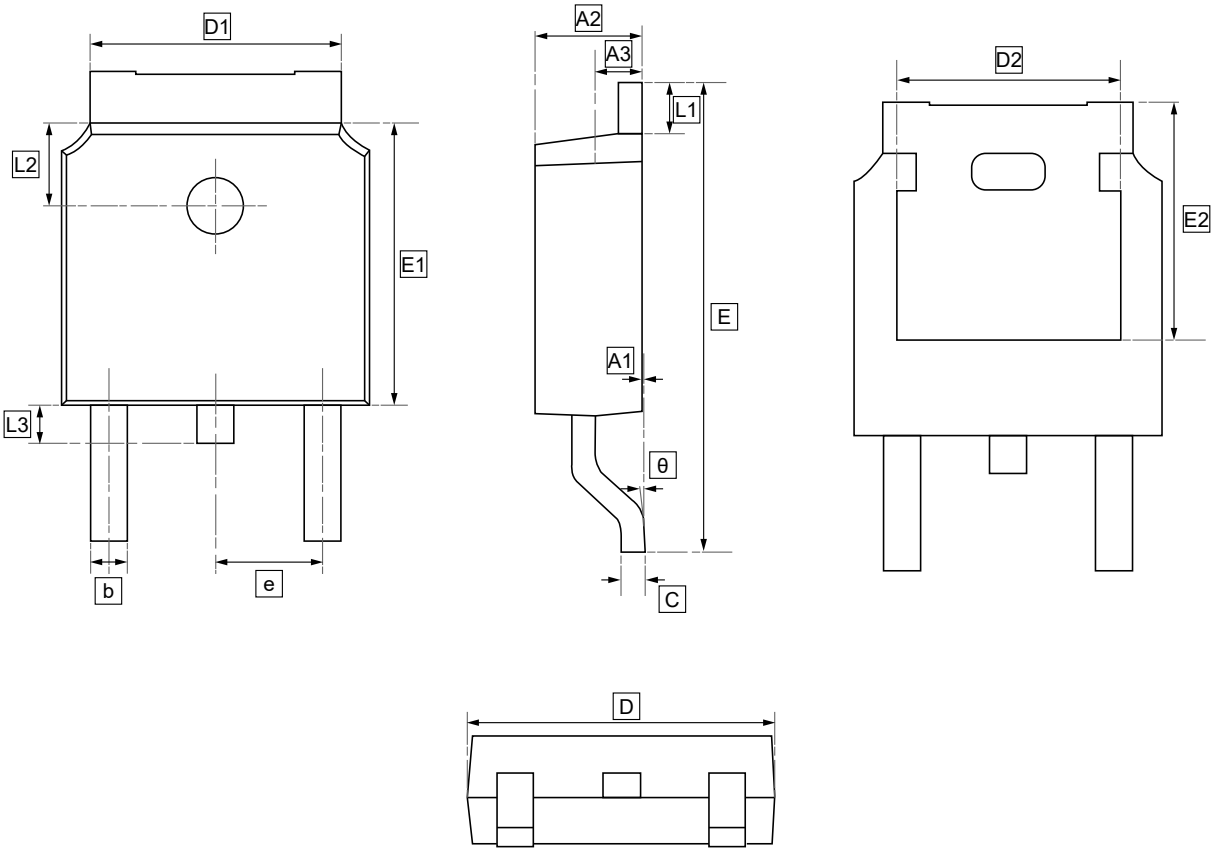


Fig 16. Gate charge waveforms

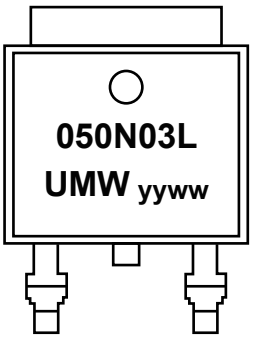
6.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

7.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IPD050N03LGATMA1	TO-252	2500	Tape and reel

8.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.