UMW IPD088N06N3G

60V N-Channel MOSFET

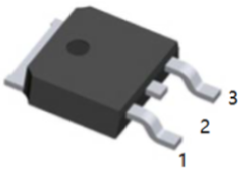
1.Features

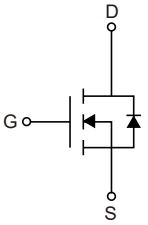
- $V_{DS\ (V)}$=60V
- I_D=50A
- $R_{DS(ON)}$<8.8mΩ(V_{GS}=10V)
- Deal for high frequency switching
- Optimized technology for DC / DC converters
- Excellent gate charge x $R_{DS(ON)}$ product (FOM)
- Very low on-resistance $R_{DS(ON)}$

2.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252





3.Absolute Maximum Ratings T_J= 25°C

Parameter	Symbol	Conditions	Value	Units
Continuous drain current	I_D	T_C=25°C[2]	50	A
		T_C=100°C	47	A
Pulsed drain current [3]	$I_{D,pulse}$	T_C=25°C	200	A
Avalanche current, single pulse [4]	E_{AS}	I_D=50A, R_{GS}=25Ω	43	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	T_C=25°C	71	W
Storage temperature	T_J,T_{STG}		-55 to 175	°C
IEC cimatic category; DIN IEC 68-1			55/175/56	

Notes:

[1] J-STD 20 and JESD 22.

[2] Currentislimited by bondwire; with an R_{thJC}=2.1K/W the chip is able to carry 67A .

[3] See figure 3 for more detailed information

[4] See figure 13 for more detailed information.

4.Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Thermal resistance, junction -case	R_{thJC}				2.1	K/W
Thermal resistance, junction -ambient	R_{thJA}	minimal footprint			62	K/W
		6 cm^2 cooling area [4])			40	K/W
Drain-source breakdown voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=1mA	60			V
Gate threshold voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=34μA	2	3	4	V
Zero gate voltage drain current	I_{DSS}	V_{DS}=60V, V_{GS}=0V, T_J=25°C		0.1	1	μA
		V_{DS}=60V, V_{GS}=0V, T_J=125°C		10	100	μA
Gate-source leakage current	I_{GSS}	V_{GS}=20V, V_{DS}=0V		1	100	nA
Drain-source on-state resistance [5])	$R_{DS(ON)}$	V_{GS}=10V, I_D=50A		7.1	8.8	mΩ
Gate resistance	R_G			0.9		Ω
Transconductance	g_{FS}	$\|V_{DS}\|>2\|I_D\|R_{DS(ON)max}$,$I_D$=50A	29	57		S
Input capacitance	C_{iss}	V_{GS}=0V, V_{DS}=30V, f=1MHz		2900	3900	pF
Output capacitance	C_{oss}			640	850	pF
Reverse transfer capacitance	C_{rss}			23		pF
Turn-on delay time	$t_{D(on)}$	V_{DD}=30V, V_{GS}=10V I_D=45A, R_G=3.5Ω		15		ns
Rise time	t_r			40		ns
Turn-off delay time	$t_{D(off)}$			20		ns
Fall time	t_f			5		ns
Gate to source charge	Q_{gs}	V_{DD}=30V, I_D=50A V_{GS}=0 to 10V		16		nC
Gate to drain charge	Q_{gd}			3		nC
Switching charge	Q_{SW}			11		nC
Gate charge total	Q_g			36	48	nC
Gate plateau voltage	$V_{plateau}$			5.6		V

Output charge	Q_{oss}	V_{DD}=30V, V_{GS}=0V		29	38	nC
Diode continous forward current	I_S	T_C=25°C			50	A
Diode pulse current	$I_{S,pulse}$				200	A
Diode forward voltage	V_{SD}	V_{GS}=0V, I_F=50A, T_J=25°C		1	1.2	V
Reverse recovery time	t_{rr}	V_R=30V, I_F=45A, di_F/dt=100A/μs		45		ns
Reverse recovery charge	Q_{rr}			40		nC

Notes:

[4] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer , 70 um thick) copper area for drainconnection . PCB is vertical in still air.

[5] See figure 16 for gate charge parameter definition

5.1Typical characteristic

$P_{tot}=f(T_C)$

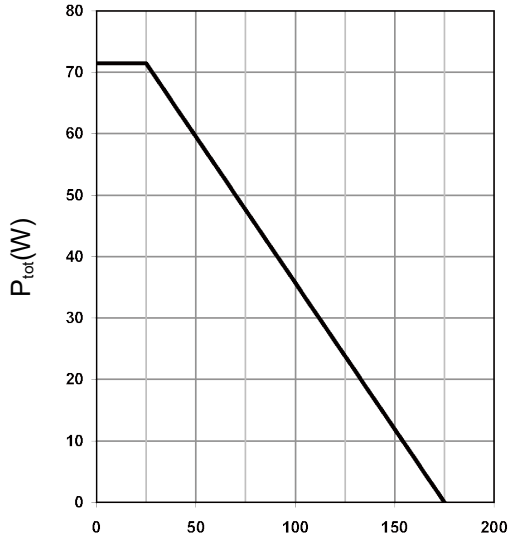


Fig 1. Power dissipation

$I_D=f(T_C)$; $V_{GS}\geq 10V$

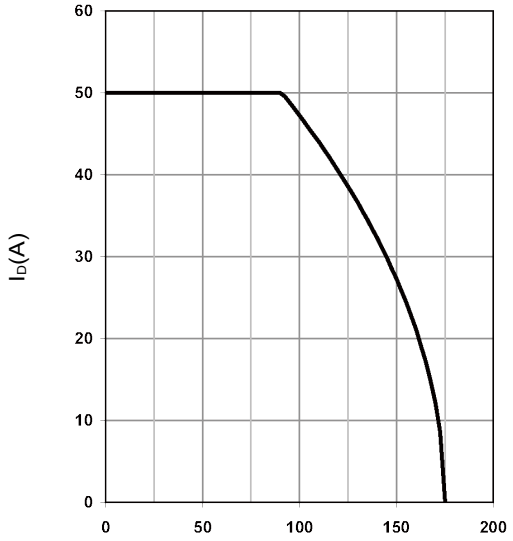


Fig 2. Drain current

ID=f(V_{DS}); T_C=25°C; D=0; parameter: t_p

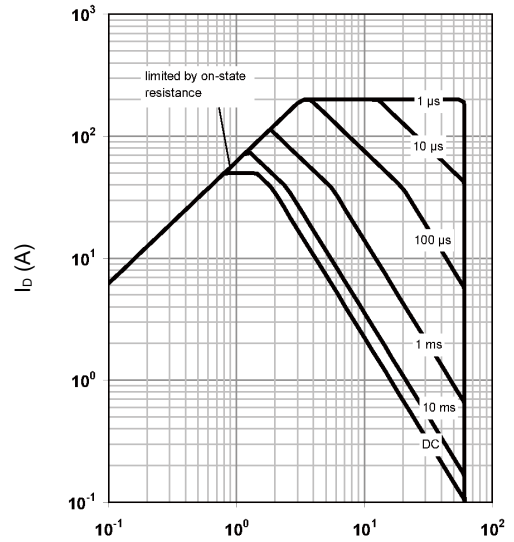


Fig 3. Safe operating area

$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

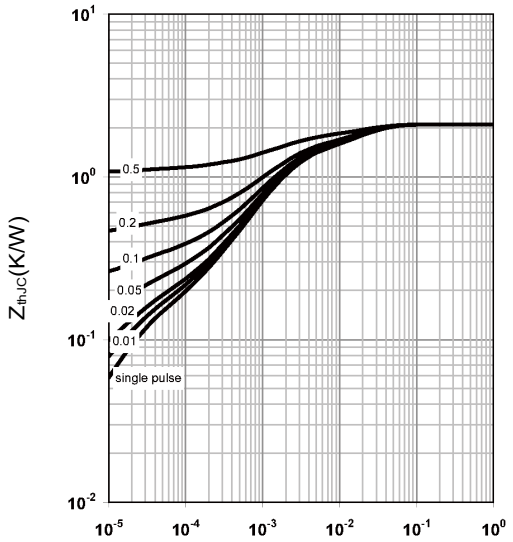


Fig 4. Max transient thermal impedance

5.2Typical characteristic

$I_D=f(V_{DS})$; T_J=25°C; parameter: V_{GS}

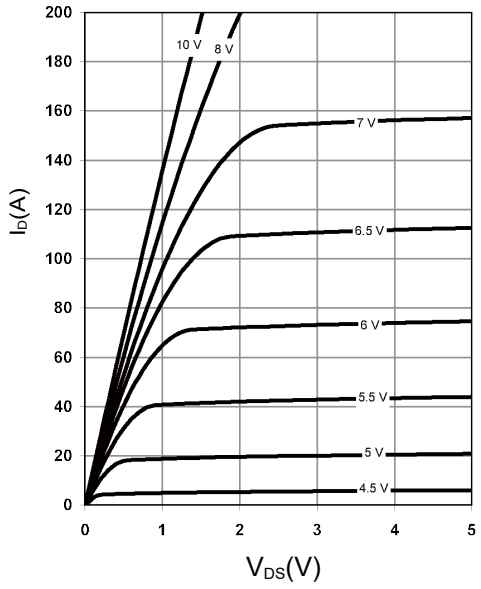


Fig 5. output characteristics

$R_{DS(ON)}=f(I_D)$; T_J=25°C; parameter: V_{GS}

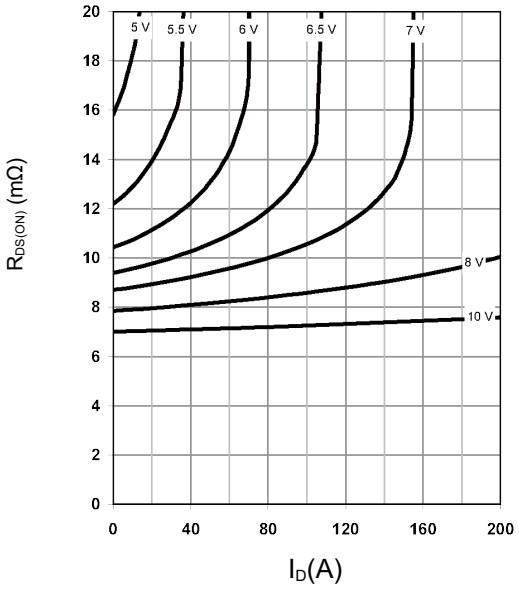


Fig 6. drain-source on resistance

$ID=f(V_{GS})$; $|V_{DS}|>2|\ I_D\ |R_{DS(ON)max}$; parameter: T_J

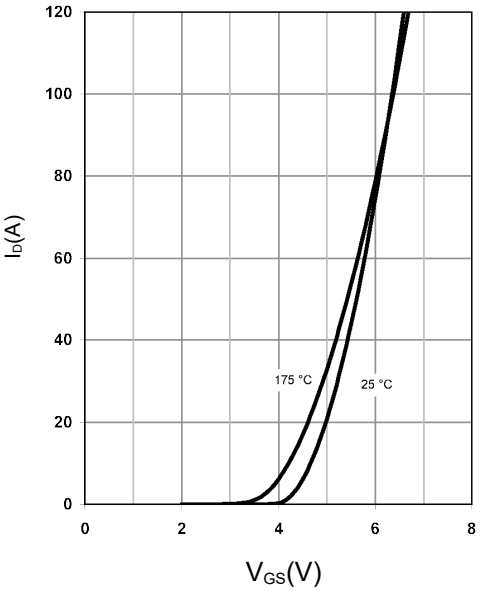


Fig 7. transfer characteristics

$g_{fs}=f(I_D)$; T_J=25°C

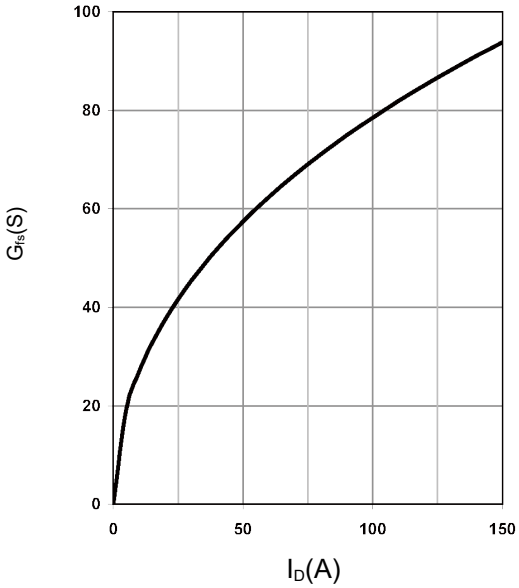


Fig 8. forward transconductance

5.3Typical characteristic

$R_{DS(ON)}=f(T_J)$; I_D=50A; V_{GS}=10V

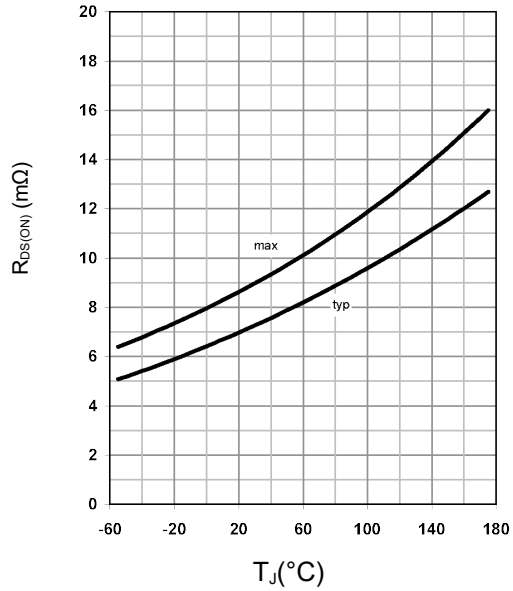


Fig 9. Drain-source on-state resistance

$V_{GS(th)}=f(T_J)$; $V_{GS}=V_{DS}$; parameter: I_D

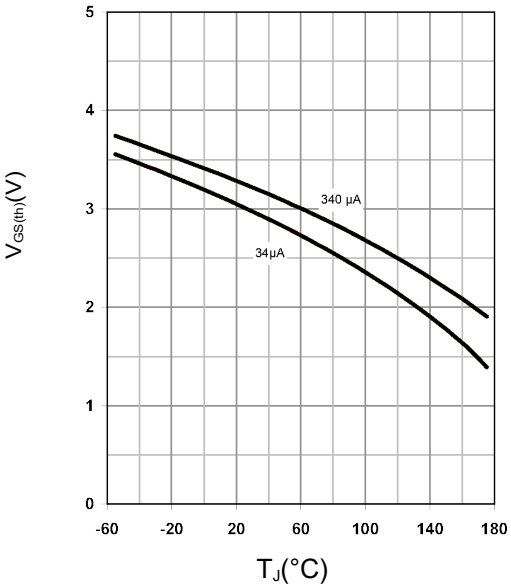


Fig 10. Gate threshold voltage

C=f(V_{DS}); V_{GS}=0V; f=1MHZ

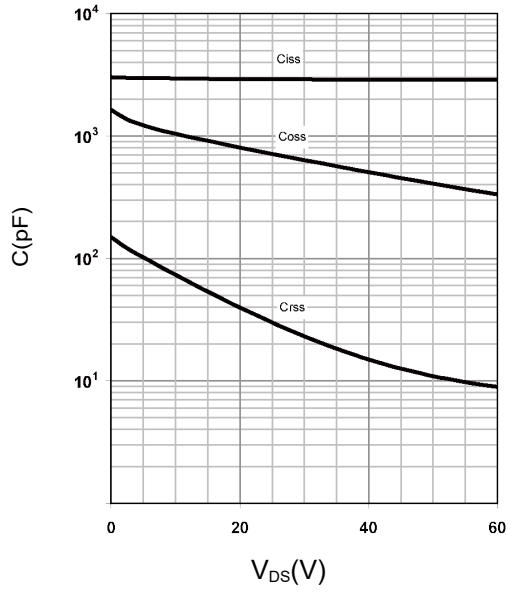


Fig 11. capacitances

$I_F=f(V_{SD})$; parameter: T_J

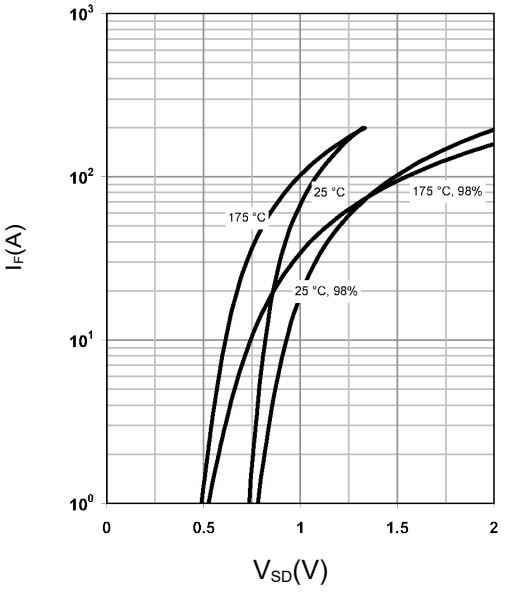


Fig 12. Forward characteristics of reverse diode

5.4Typical characteristic

$I_{AS}=f(t_{AV})$; $R_{GS}=25\Omega$; parameter: $T_{j(start)}$

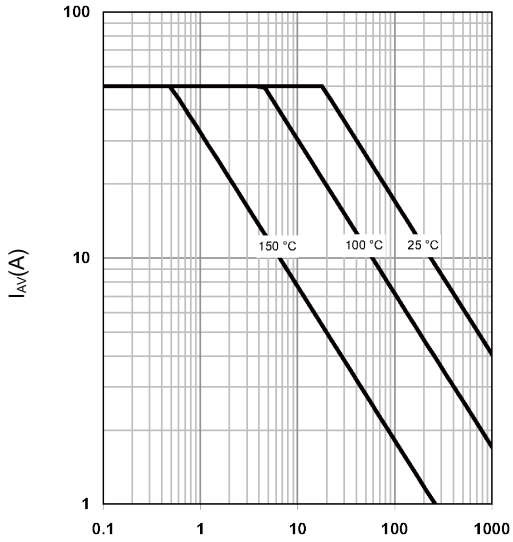


Fig 13. Avalanche characteristics

$V_{GS}=f(Q_{gate})$; $I_D=50A$ pulsed; parameter: V_{DD}

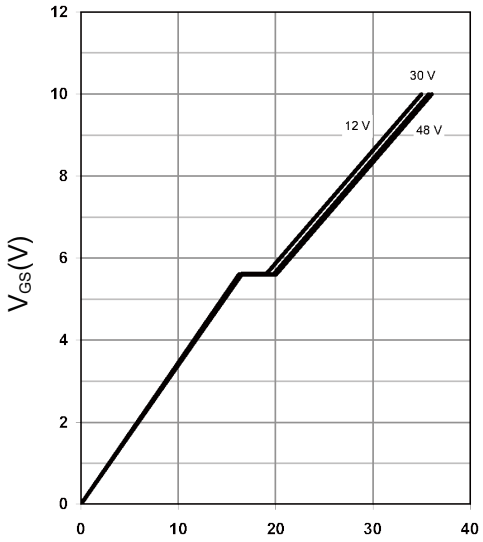


Fig 14. gate charge

$V_{BR(DSS)}=f(T_J)$; $I_D=1mA$

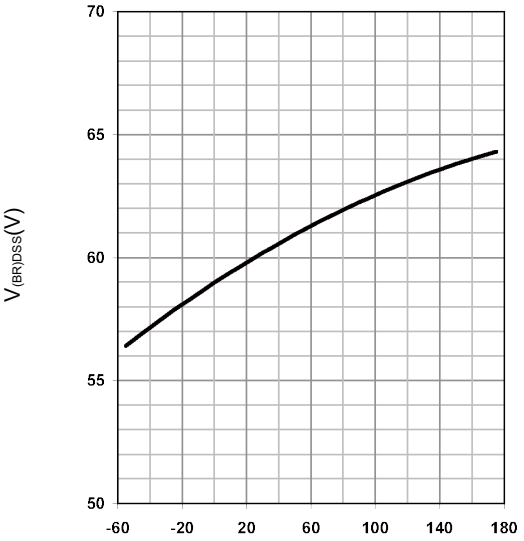


Fig 15. drain source breakdown voltage

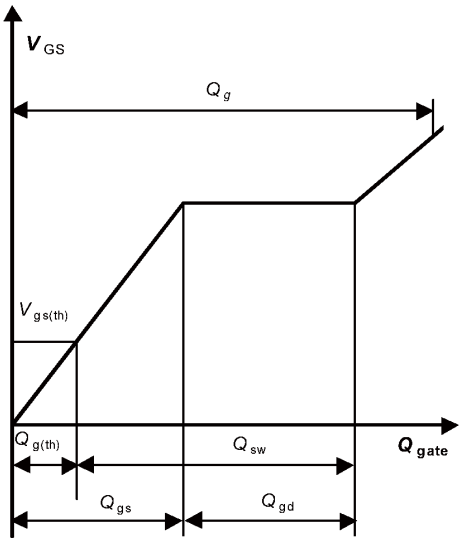
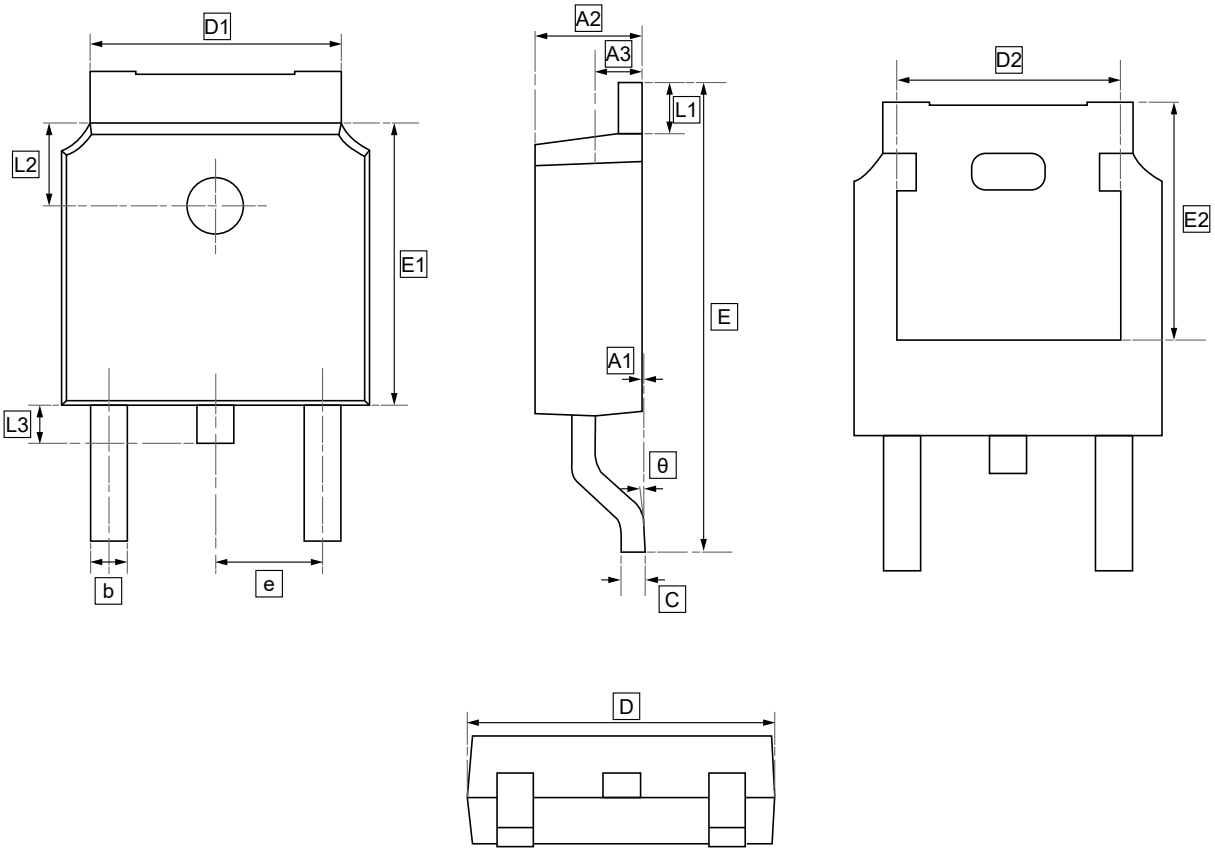


Fig 16. Gate charge waveforms

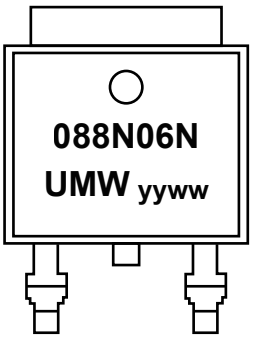
6.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

7.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IPD088N06N3G	TO-252	2500	Tape and reel

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