UMW IRF7406TR

-30V P-Channel MOSFET

1.Description

The SOP-8 has been modified throuah a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space.The package is designed for vapor phase. infra red. or wave so derina techniaues.Power dissipation of qreater than 0.8W is possible in a typical PCB mount application.

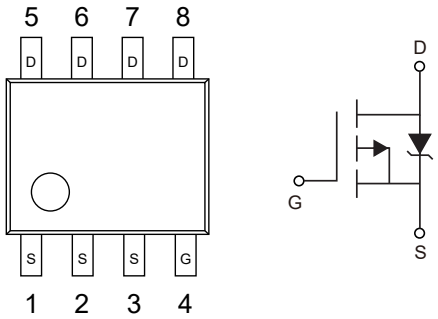
2.Features

- Generation VTechnology
- Ultra Low On-Resistance
- P-Channel Mosfet
- Surface Mount
- Available in Tape&Reel
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free

3.Pinning information

Pin	Symbol	Description
1,2,3	S	SOURCE
4	G	GATE
5,6,7,8	D	DRAIN

SOP-8



4.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
10 Sec. Pulsed Drain Current, V_{GS}=-10V	T_A=25°C	I_D	-6.7	A
Continuous Drain Current, V_{GS}=-10V	T_A=25°C		-5.8	A
Continuous Drain Current, V_{GS}=-10V	T_A=70°C		-3.7	A
Pulsed Drain Current ①		I_{DM}	-23	A
Power Dissipation	T_A=25°C	P_D	2.5	W
Linear Derating Factor			0.02	W/°C
Gate-to-Source Voltage		V_{GS}	±20	V
Peak Diode Recovery dv/dt ②		dv/dt	-5	V/ns
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

5.Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ④	$R_{\theta JA}$		50	°C/W

6.Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=-250μA, V_{GS}=0V	-30			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D=-1mA,Reference to 25°C		-0.02		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-2.8A ③			45	mΩ
		V_{GS}=-4.5V, I_D=-2.4A ③			70	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1			V
Forward Transconductance	g_{FS}	V_{DS}=-15V, I_D=-2.8A	3.1			S
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=-24V, V_{GS}=0V			-1	μA
		V_{DS}=-24V,V_{GS}=0V,T_J=125°C			-25	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=-20V			-100	nA
Gate-to-Source Reverse Leakage		V_{GS}=20V			100	
Total Gate Charge	Q_g	I_D=-2.8A			59	nC
Gate-to-Source Charge	Q_{gs}	V_{DS}=-2.4V, V_{GS}=-10V			5.7	
Gate-to-Drain ("Miller") Charge	Q_{gd}	See Fig. 6 and 12 ③			21	
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=-15V		16		ns
Rise Time	t_r	I_D=-2.8A		33		ns
Turn-Off Delay Time	$t_{D(off)}$	R_G=6Ω		45		ns
Fall Time	t_f	R_D=5.3Ω, See Fig. 10 ③		47		ns
Internal Drain Inductance	L_D	Between lead tip		2.5		nH
Internal Source inductance	L_S	and center of die contact		4		
Input Capacitance	C_{iss}	V_{GS}=0V		1100		pF
Output Capacitance	C_{oss}	V_{DS}=-25V		490		pF
Reverse Transfer Capacitance	C_{rss}	f=1.0MHz, See Fig.5		220		pF

Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			-3.1	A
Pulsed Source Current (Body Diode) ①	I_{SM}				-23	
Diode Forward Voltage	V_{SD}	T_J=25°C,I_S=-2A,V_{GS}=0V ③			-1	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=-2.8A		42	63	ns
Reverse Recovery Charge	Q_{rr}	dI/dt=100A/μs ③		64	96	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

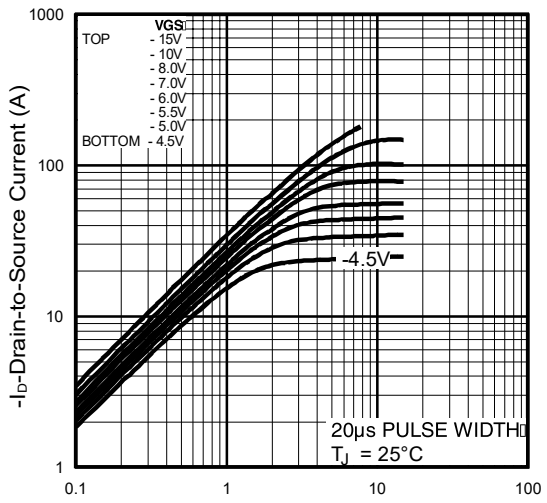
① Repetitive rating; pulse width limited by max.junction temperature.(See fig.11)

② I_{SD}≤ -2.8A, di/dt ≤90A/μs, V_{DD}≤ $V_{(BR)DSS}$,T_J≤ 150°C.

③ Pulse width ≤ 300μs; duty cycle ≤ 2%.

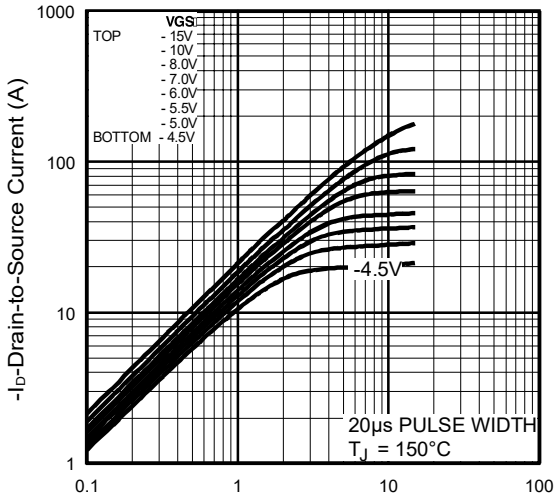
④ Surface mounted on FR-4 board, t ≤ 10sec.

7.1Typical Characterisitics



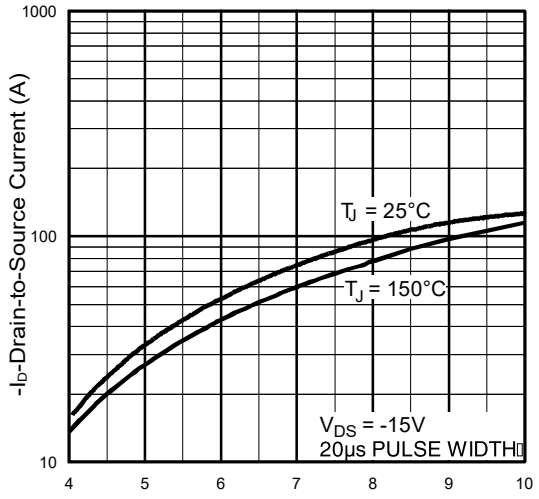
-V_{DS} - Drain-to-Source Voltage (V)

Fig 1. Typical Output Characteristics



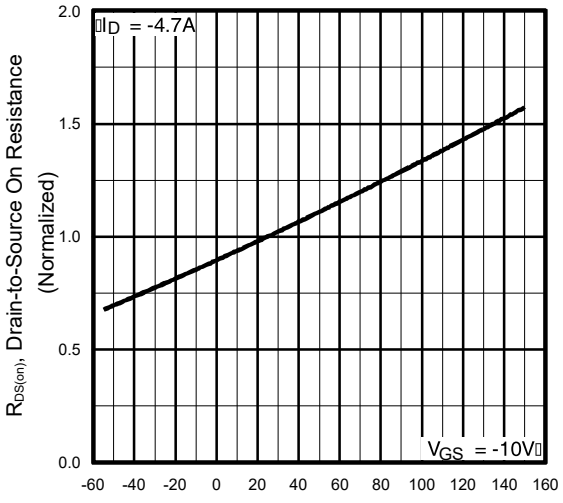
-V_{DS} - Drain-to-Source Voltage (V)

Fig 2. Typical Output Characteristics



-V_{GS}, Gate-to-Source Voltage (V)

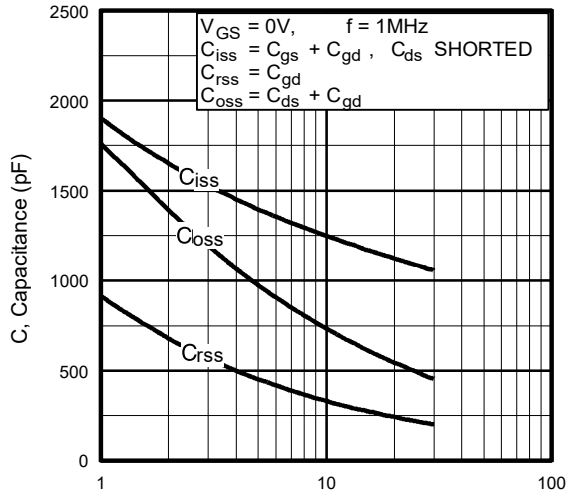
Fig 3. Typical Transfer Characteristics



T_J, Junction Temperature (°C)

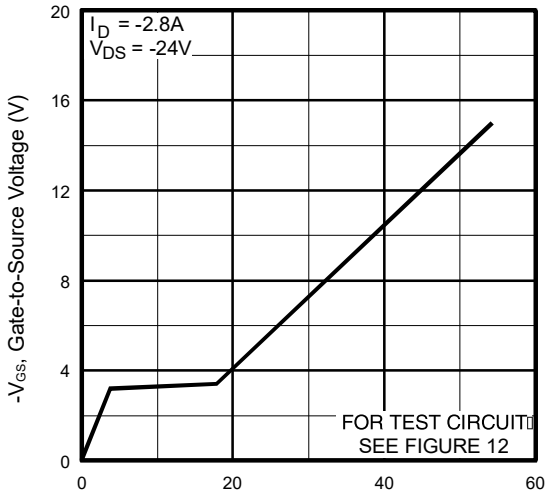
Fig 4. Nomalized On-ResistanceVs. Temperature

7.2Typical Characterisitics



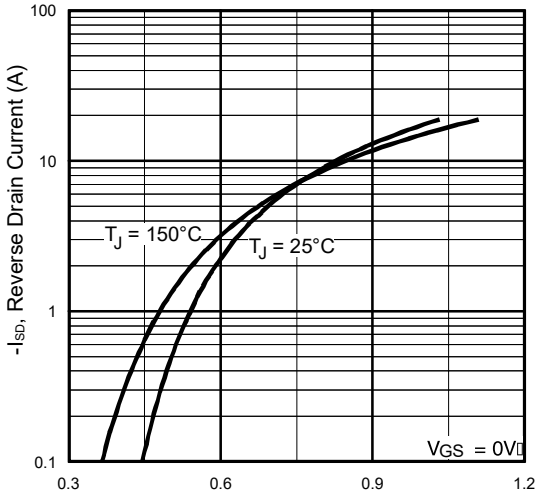
-V_{DS} ,Drain-to-Source Voltage (V)

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage



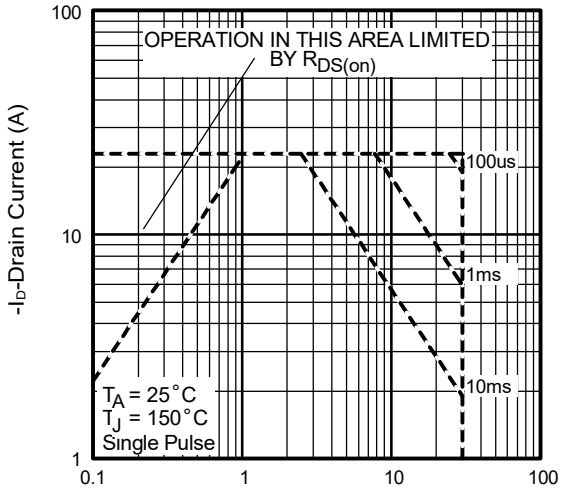
Q_G, Total Gate Charge (nC)

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage



-V_{SD}, Source-to-Drain Voltage (V)

Fig 7. Typical Source-Drain Diode Forward Voltage



-V_{DS}, Drain-to-Source Voltage (V)

Fig 8. Maximum Safe Operating Area

7.3Typical Characterisitics

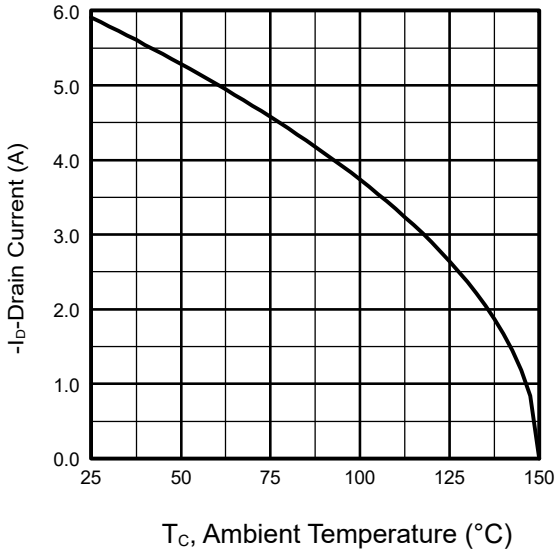


Fig 9. Maximum Drain Current Vs.AmbientTemperature

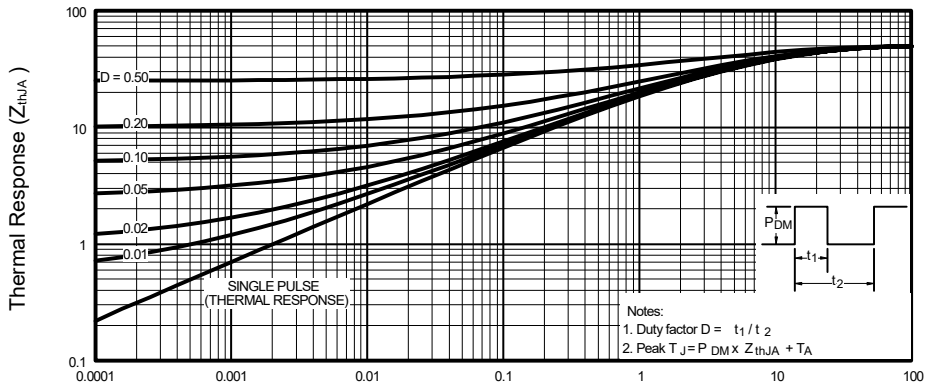


Fig 10. Maximum Effective Transient Themal Impedance, Junction-to-Ambient

7.4Typical Characterisitics

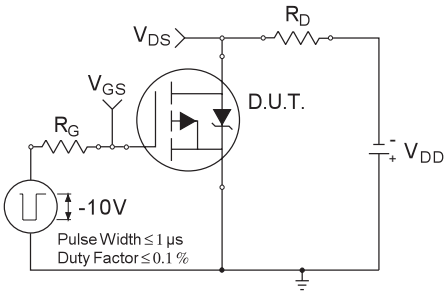


Fig 11a. Switching Time Test Circuit

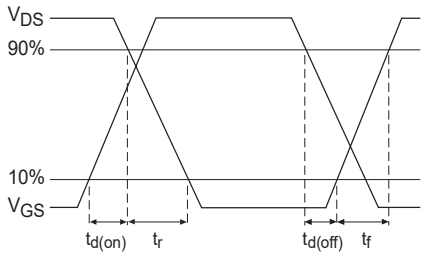


Fig 11b. Switching Time Waveforms

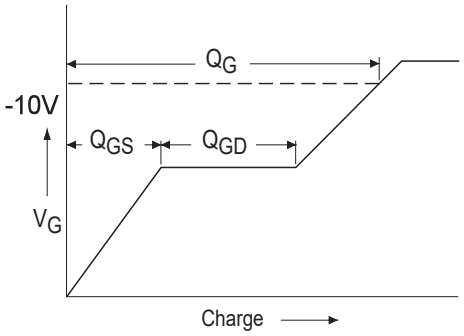


Fig 12a. Basic Gate Charge Wavefomm

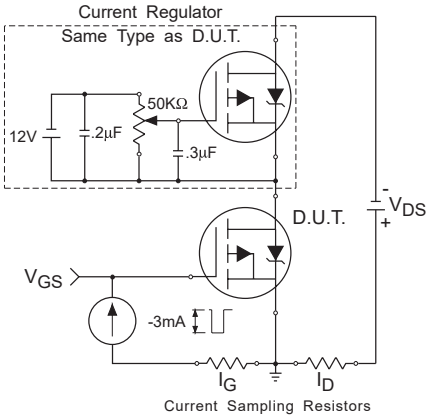
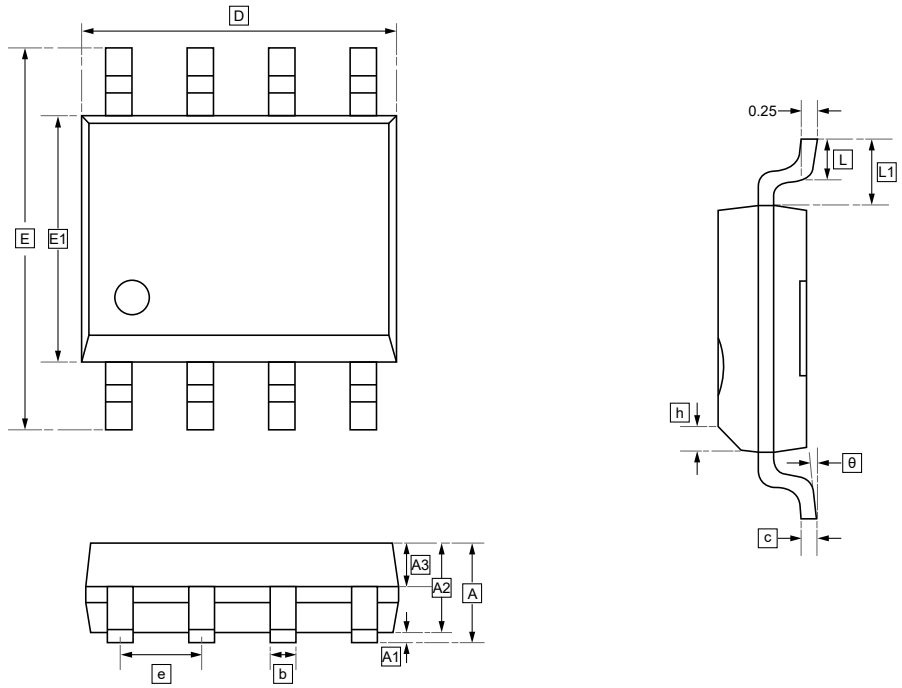


Fig 12b. Gate Charge Test Circuit

8.SOP-8 Package Outline Dimensions

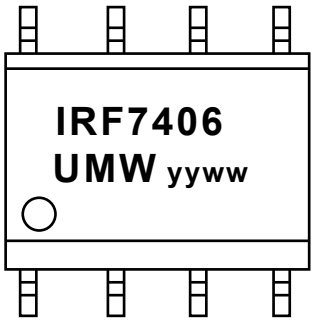


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.70	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.10	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRF7406TR	SOP-8	3000	Tape and reel

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