UMW IRFR1205TR

55V N-Channel MOSFET

1.Description

The D-PAK is designed for surface mounting using vapor phase, infrared,or wave soldering technigues. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

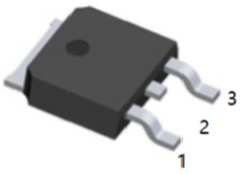
2.Features

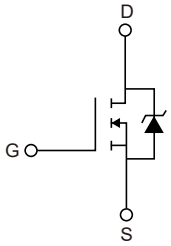
- $V_{DS\ (V)}$=55V
- I_D=44A
- $R_{DS(ON)}$<27mΩ(V_{GS}=10V)

3.Pinning information

Pin	Symbol	Description
1	G	GATE
3	S	SOURCE
2	D	DRAIN

TO-252(DPAK)
top view





4.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, V_{GS}=10V	T_C=25°C	I_D	44 ⑤	A
Continuous Drain Current, V_{GS}=10V	T_C=100°C		31 ⑤	A
Pulsed Drain Current ① ⑦		I_{DM}	160	A
Power Dissipation	T_C=25°C	P_D	107	W
Linear Derating Factor			0.71	W/°C
Gate-to-Source Voltage		V_{GS}	±20	V
Single Pulse Avalanche Energy ② ⑦		E_{AS}	210	mJ
Avalanche Current ① ⑦		I_{AR}	25	A
Repetitive Avalanche Energy ① ⑦		E_{AR}	11	mJ
Peak Diode Recovery dv/dt ③		dv/dt	5	V/ns
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C
Soldering Temperature, for 10 seconds			300 (1.6mm from case)	°C

5.Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Junction-to-Case	$R_{\theta JC}$		1.4	°C/W
Junction-to-Ambient (PCB Mount)	$R_{\theta JA}$		50	°C/W
Junction-to-Ambient	$R_{\theta JA}$		110	°C/W

6.Electrical Characteristics @ T_J= 25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=250μA, V_{GS}=0V	55			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D=1mA,Reference to 25°C		0.055		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=26A ④			27	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2		4	V
Forward Transconductance	g_{FS}	V_{DS}=25V, I_D=25A ⑦	17			S
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=55V, V_{GS}=0V			25	μA
		V_{DS}=44V,V_{GS}=0V,T_J=150°C			250	μA
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=20V			100	nA
Gate-to-Source Reverse Leakage		V_{GS}=-20V			-100	nA
Total Gate Charge	Q_g	I_D=25A			65	nC
Gate-to-Source Charge	Q_{gs}	V_{DS}=44V, V_{GS}=10V			12	nC
Gate-to-Drain ("Miller") Charge	Q_{gd}	See Fig. 6 and 13 ④ ⑦			27	nC
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=28V, I_D=25A		7.3		ns
Rise Time	t_r	R_G=12Ω, R_D=1.1Ω		69		ns
Turn-Off Delay Time	$t_{D(off)}$	See Fig. 10 ④ ⑦		47		ns
Fall Time	t_f			60		ns
Internal Drain inductance	L_D	Between lead, 6mm (0.25in.)from package and center of die contact ⑥		4.5		nH
Internal Source inductance	L_S			7.5		nH
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=25V		1300		pF
Output Capacitance	C_{oss}	f = 1.0MHz, See Fig. 5 ⑦		410		pF
Reverse Transfer Capacitance	C_{rss}			150		pF

Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			44 ⑤	A
Pulsed Source Current (Body Diode) ①⑦	I_{SM}				160	
Diode Forward Voltage	V_{SD}	T_J=25°C, I_S=22A, V_{GS}=0V ④			1.3	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=25A dI/dt=100A/μs ④⑦		65	98	ns
Reverse Recovery Charge	Q_{rr}			160	240	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD}=25V, starting T_J=25°C, L=470μH, R_G=25Ω, I_{AS}=25A. (See Figure 12)

③ I_{SD} ≤25A, di/dt ≤320A/μs, V_{DD} ≤ $V_{(BR)DSS}$,T_J ≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%

⑤ Calculated continuous current based on maximum allowable junctiontemperature:Package limitation current = 20A

⑥ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact.

⑦ Uses IRFZ44N data and test conditions.

7.1Typical Characterisitics

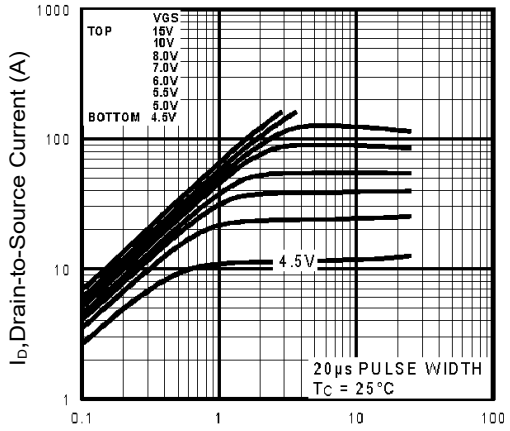


Figure 1: Typical Output Characteristics

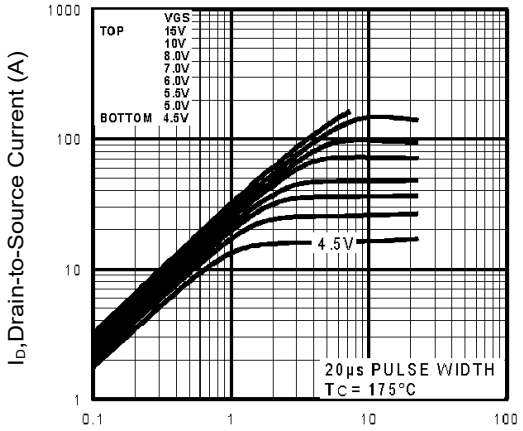


Figure 2: Typical Output Characteristics

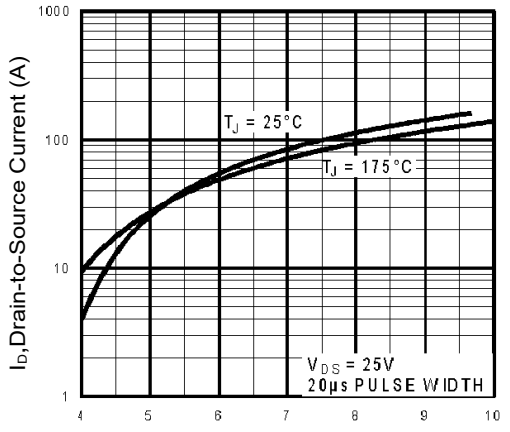


Figure 3: Typical Transfer Characteristics

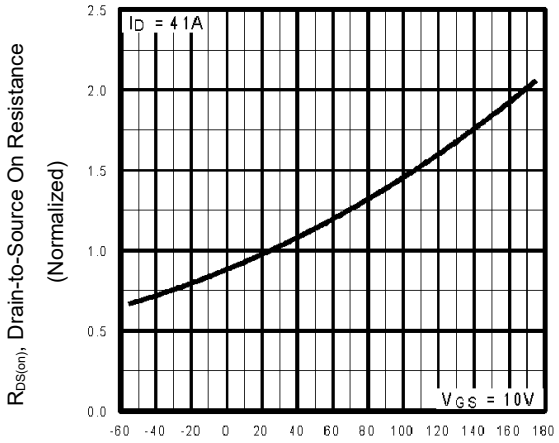
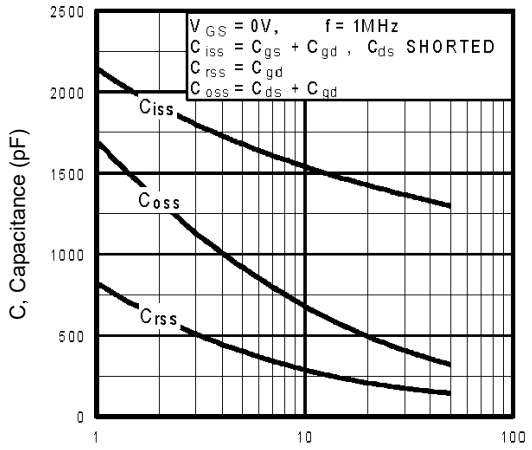


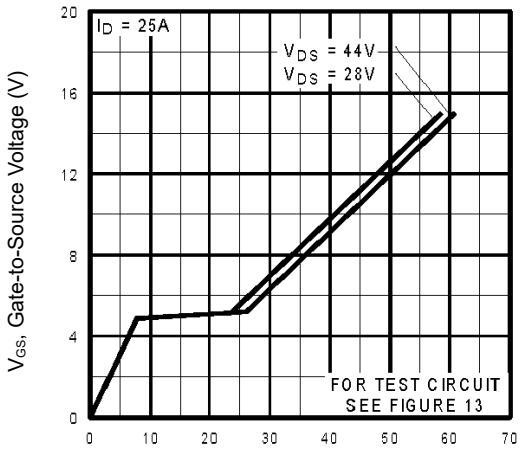
Figure 4: Nomalized On-ResistanceVs. Temperature

7.2Typical Characterisitics



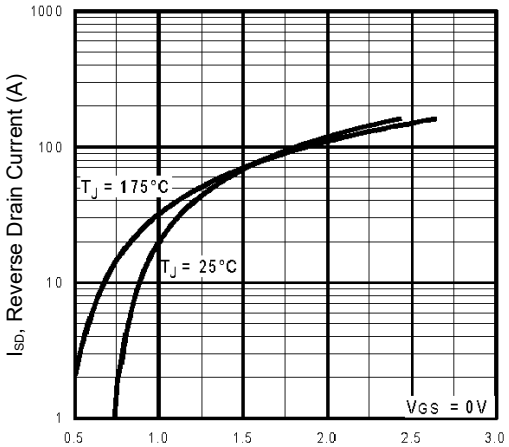
V_{DS} ,Drain-to-Source Voltage (V)

Figure 5: Typical Capacitance Vs. Drain-to-Source Voltage



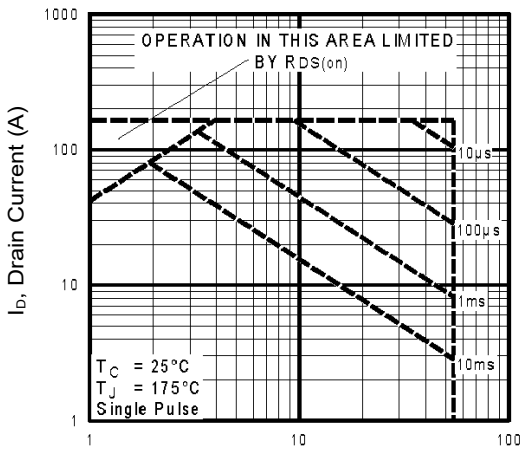
Q_G, Total Gate Charge (nC)

Figure 6: Typical Gate Charge Vs. Gate-to-Source Voltage



V_{SD}, Source-to-Drain Voltage (V)

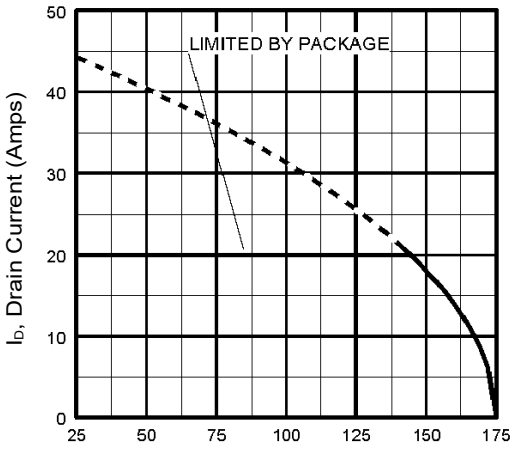
Figure 7: Typical Source-Drain Diode Forward Voltage



V_{DS}, Drain-to-Source Voltage (V)

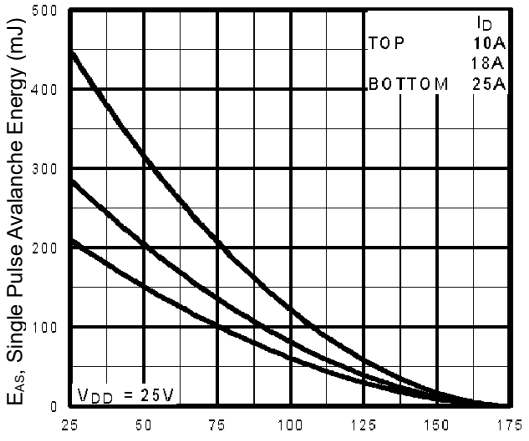
Figure 8: Maximum Safe Operating Area

7.3Typical Characterisitics



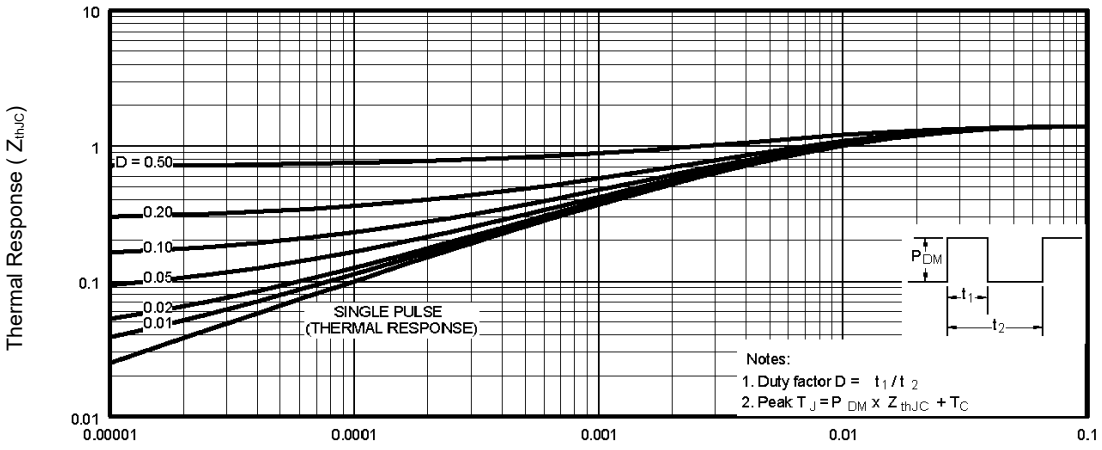
T_C, Case Temperature (°C)

Figure 9: Maximum Drain Current Vs. Case Temperature



Starting T_J, Junction Temperature (°C)

Figure 10: Maximum Avalanche Energy Vs. Drain Current



t_1 , Rectangular Pulse Duration (sec)

Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

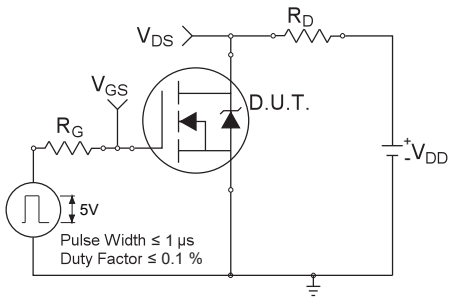


Figure 12a: Switching Time Test Circuit

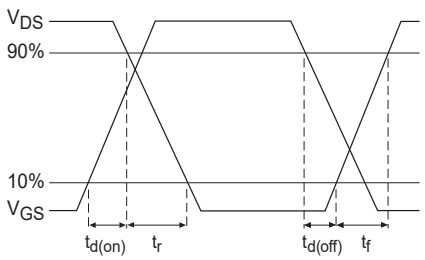


Figure 12b: Switching Time Waveforms

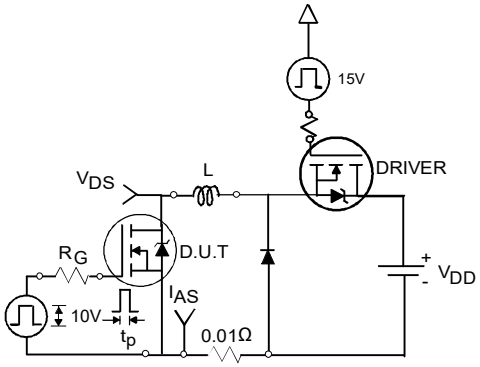


Figure 13a: Unclamped Inductive Test Circuit

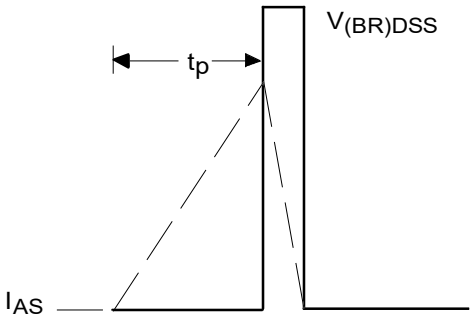


Figure 13b: Unclamped Inductive Waveforms

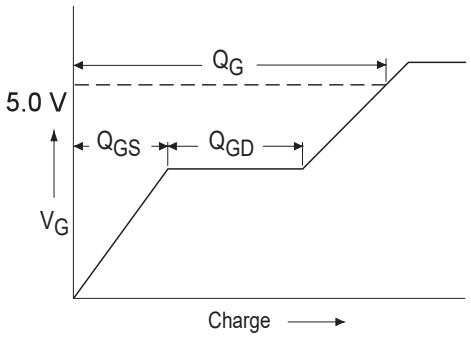


Figure 14a: Basic Gate Charge Waveform

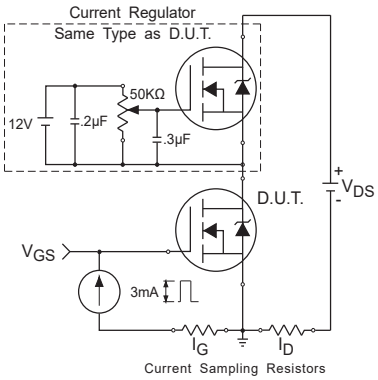
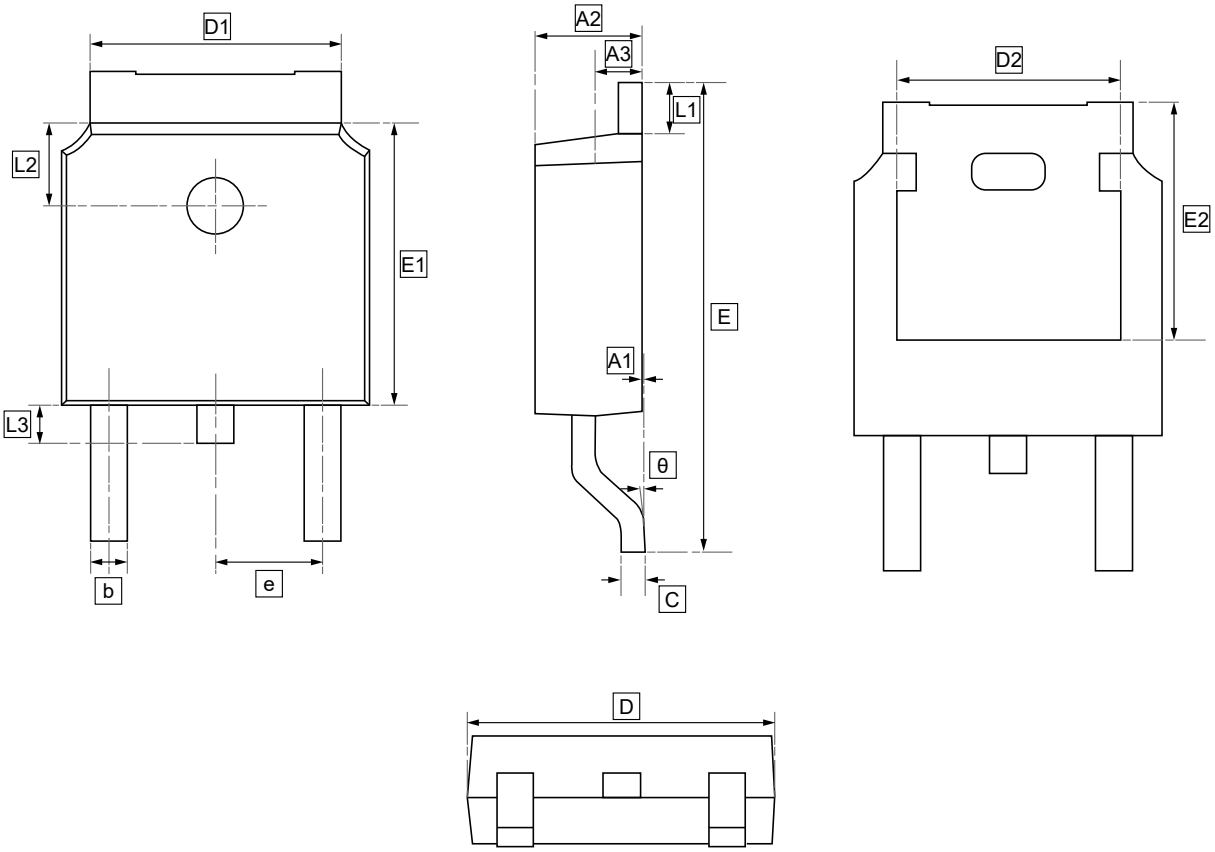


Figure 14b: Gate Charge Test Circuit

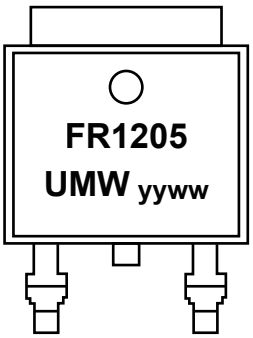
8.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRFR1205TR	TO-252	2500	Tape and reel

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