UMW IRFR9120NTR

-100V P-Channel MOSFET

1.Description

The uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications.It is ESD protested.

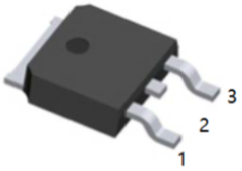
2.Features

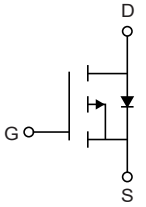
- $V_{DS\ (V)}$=-100V, I_D=-8A
- $R_{DS(ON)}$<210mΩ(V_{GS}=-10V) (Typ:145m)
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density celldesign for ultra low on-resistance

3.Pinning information

Pin	Symbol	Description
1	G	GATE
3	S	SOURCE
2	D	DRAIN

TO-252(DPAK)
top view





4.Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DS}	-100	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current-Continuous	I_D	-8	A
Drain Current-Continuous(T_C=100°C)	I_D(100°C)	-6	A
Pulsed Drain Current	I_{DM}	-30	A
Maximum Power Dissipation	P_D	40	W
Derating factor		0.32	W/°C
Single pulse avalanche energy (Note 5)	E_{AS}	110	mJ
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

5.Thermal resistance rating

Thermal Resistance,Junction-to-Case (Note 2)	R_{thJC}		3.13	°C/W

6.Electrical Characteristics @ T_J= 25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=-250μA	-100			V
Zero Gate Voltage Drain Curent	I_{DSS}	V_{DS}=-100V, V_{GS}=0V			-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1		-3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-6A		210	235	mΩ
Forward Transconductance	g_{FS}	V_{GS}=-15V, I_D=-5A	12			S
Input Capacitance	C_{iss}	V_{DS}=-25V,V_{GS}=0V,F=1MHz		760		pF
Output Capacitance	C_{oss}			260		pF
Reverse TransferCapacitance	C_{rss}			170		pF
Turn-on Delay Time	$t_{D(on)}$	V_{DD}=-50V, I_D=-10V V_{GS}=-10V, R_{GEN}=9.1Ω		14		nS
Turn-on Rise Time	t_r			18		nS
Turn-Off Delay Time	$t_{D(off)}$			50		nS
Turn-Off Fall Time	t_f			18		nS
Total Gate Charge	Q_g	V_{DS}=-50V, I_D=-4A V_{GS}=-4V		25		nC
Gate-Source Charge	Q_{gs}			5		nC
Gate-Drain Charge	Q_{gd}			7		nC
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V, I_S=-4A			-1.2	V
Diode Forward Current (Note 2)	I_S	T_J=25°C, I_F=-4A			-13	A
Reverse Recovery Time	t_{rr}			35		nS
Reverse Recovery Charge	Q_{rr}	dI/dt=100A/μs (Note3)		46		nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production
5. EAS condition： T_J=25°C,V_{DD}=-50V,V_G=-10V,L=0.5mH,R_g=25.

7.1 Typical Characterisitics

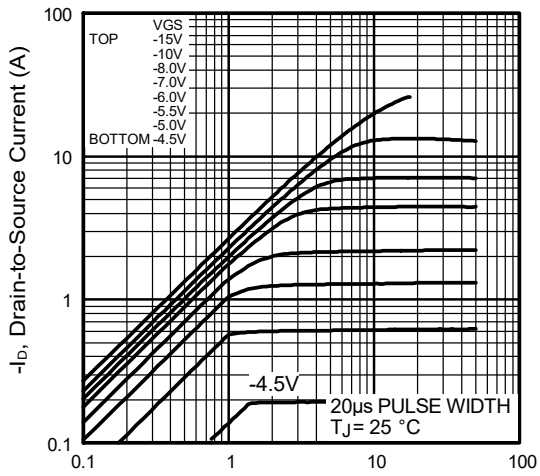


Figure 1: Typical Output CharacteriSticS

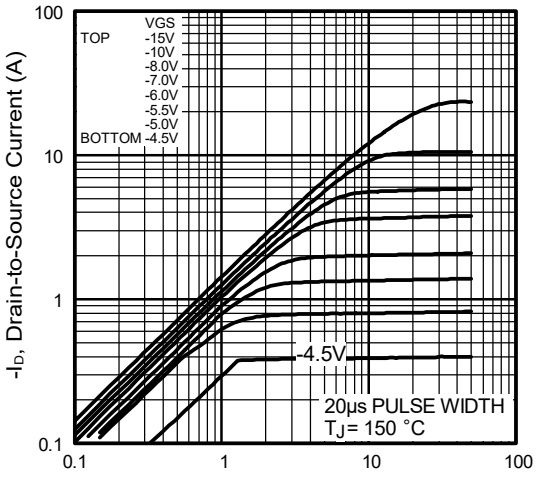


Figure 2: Typical Output CharacteriSticS

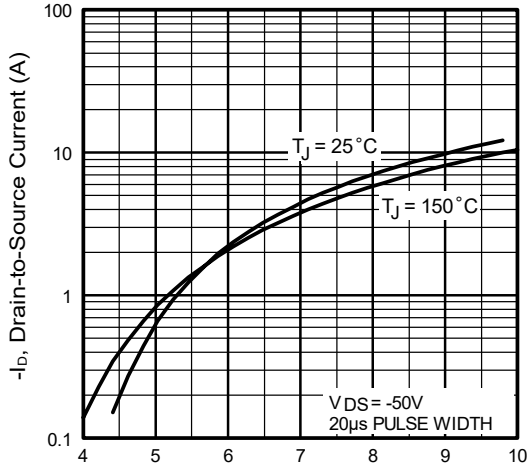


Figure 3: Typical TranSfer CharacteriSticS

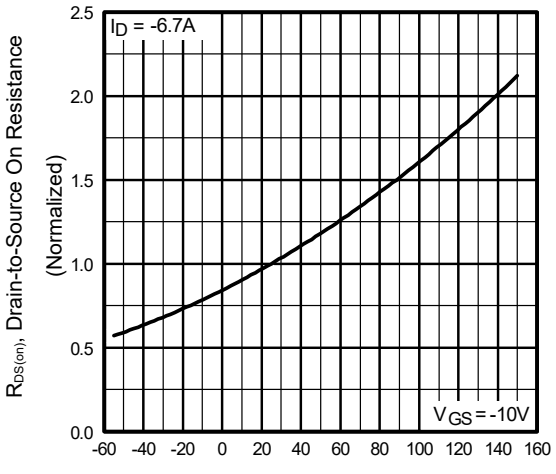
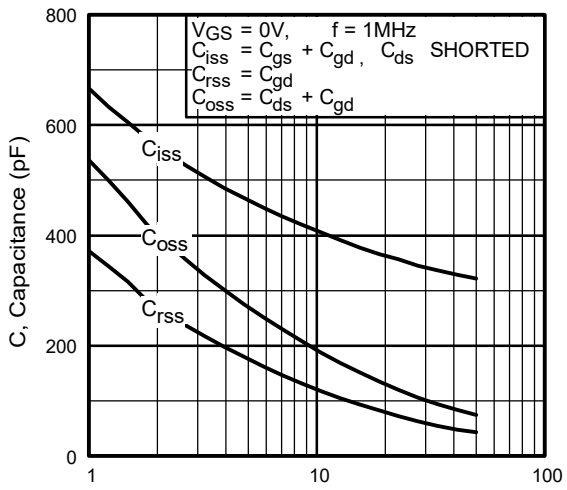


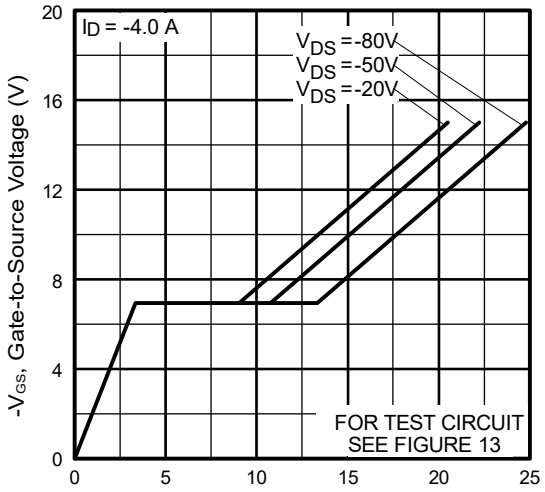
Figure 4: Normalized On-ReSiStance VS. Temperature

7.2 Typical Characterisitics



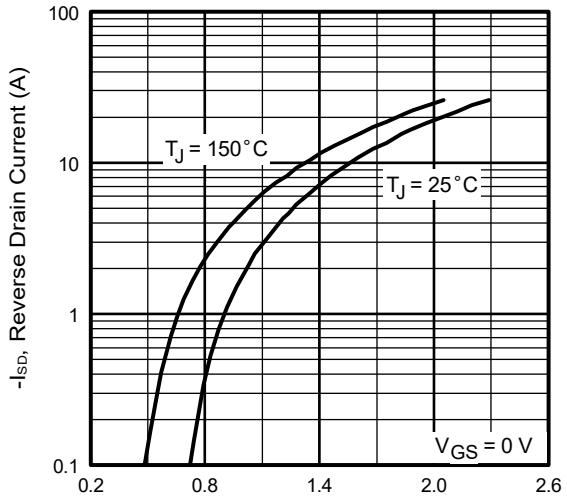
-V_{DS}, Drain-to-Source Voltage (V)

Figure 5: Typical Capacitance Vs. Drain-to-Source Voltage



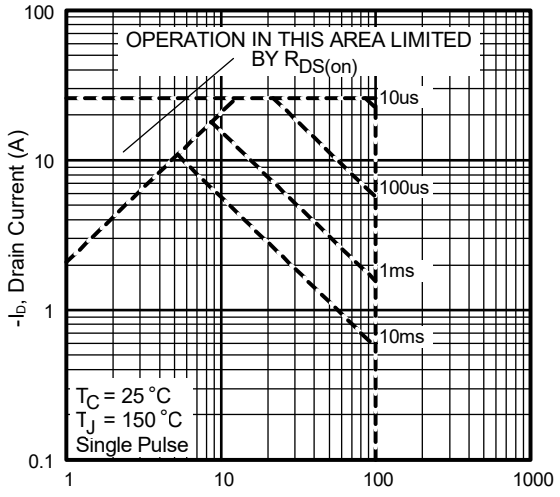
Q_G, Total Gate Charge (nC)

Figure 6: Typical Gate Charge Vs. Gate-to-Source Voltage



-V_{SD},Source- SD to-Drain Voltage (V)

Figure 7: Typical Source-Drain Diode Forward Voltage



-V_{DS}, Drain-to-Source Voltage (V)

Figure 8: Maximum Safe Operating Area

7.3 Typical Characterisitics

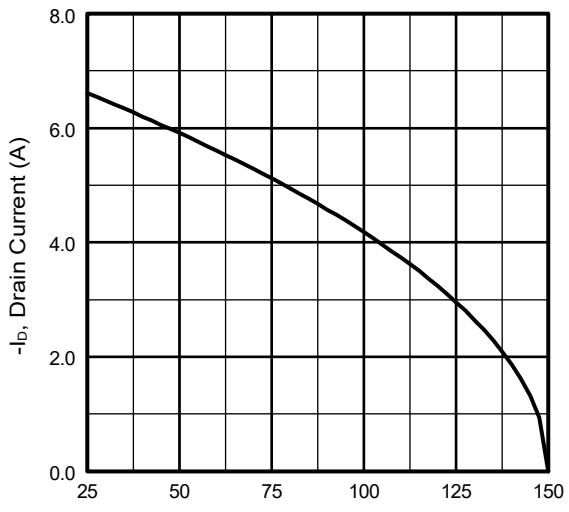


Figure 9: Maximum Drain Current Vs. Case Temperature

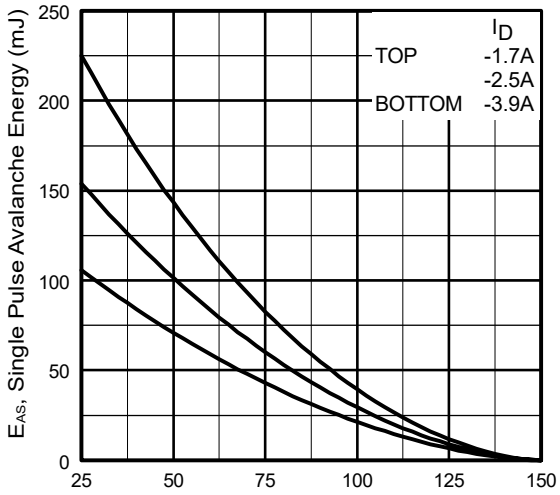


Figure 10: Maximum Avalanche Energy Vs. Drain Current

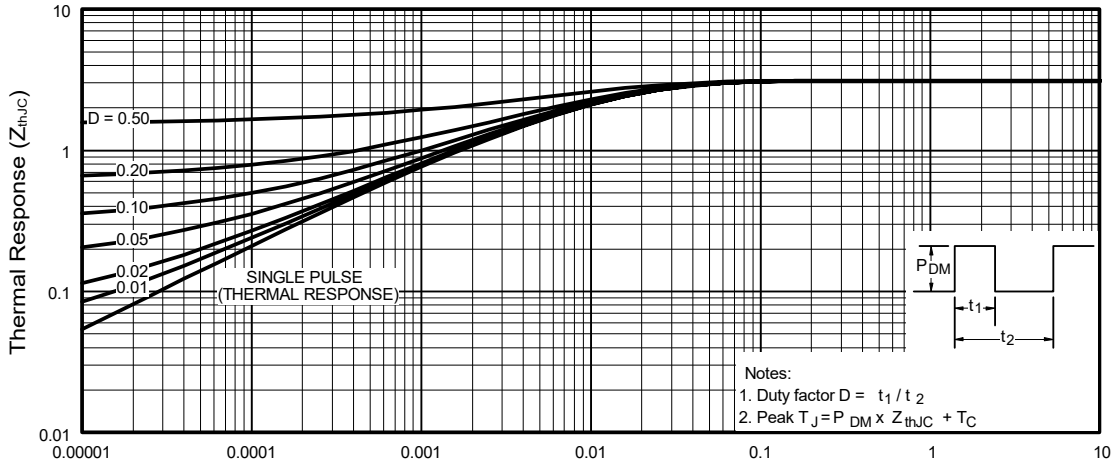
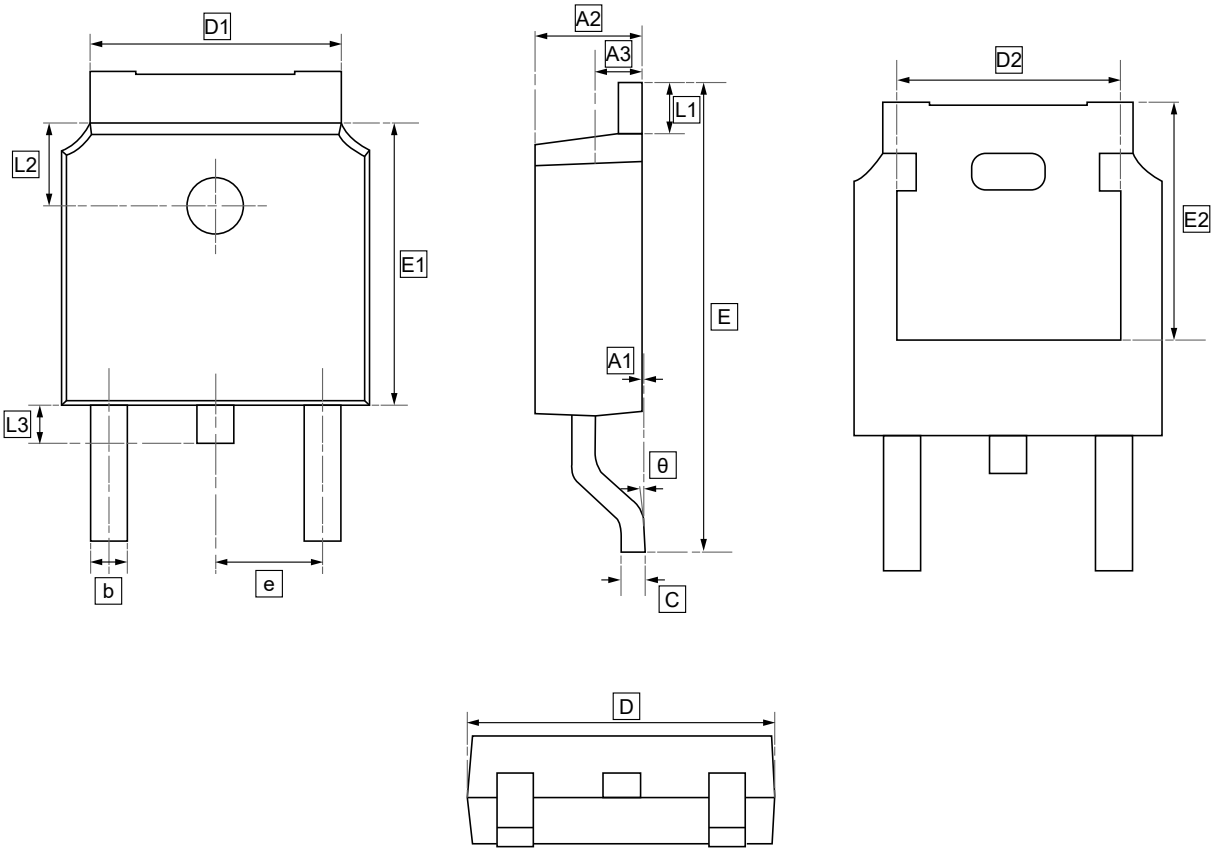


Figure 11: Maximum Effective Transient Thermal ,mpedance, JunctiOn-tO-Case

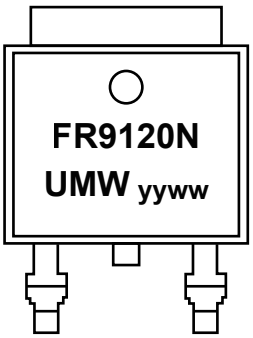
8.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRFR9120NTR	TO-252	2500	Tape and reel

10.Disclaimer

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