UMW IRFS4410Z

100V N-Channel MOSFET

1.Features

- $V_{DS\ (V)}$=100V
- I_D=97A
- $R_{DS(ON)}$<9mΩ(V_{GS}=10V)

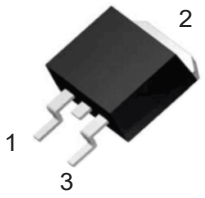
2.Applications

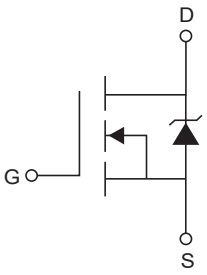
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits
- High Efficiency Synchronous Rectification in SMPS

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-263





4.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, V_{GS}=10V(Silicon Limited)	T_C=25°C	I_D	97	A
Continuous Drain Current, V_{GS}=10V(Silicon Limited)	T_C=100°C		69	A
Pulsed Drain Current ①		I_{DM}	390	A
Maximum Power Dissipation	T_C=25°C	P_D	230	W
Linear Derating Factor			1.5	W/°C
Gate-to-Source Voltage		V_{GS}	±20	V
Peak Diode Recovery ③		dv/dt	16	V/ns
Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C
Soldering Temperature, for 10 seconds(1.6mm from case)			300	°C
Mounting torque, 6-32 or M3 screw			10lb. in (1.1N. m)	
Single Pulse Avalanche Energy ②		$E_{AS(Thermally\ limited)}$	242	mJ
Avalanche Current		I_{AR}	See Fig.18, 20	A
Repetitive Avalanche Energy		E_{AR}	22a, 22b	mJ

5.Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Junction-to-Case ⑧	$R_{\theta JC}$		0.65	°C/W
Case-to-Sink, Flat Greased Surface , TO-220	$R_{\theta CS}$	0.5		°C/W
Junction-to-Ambient, TO-220 ⑧	$R_{\theta JA}$		62	°C/W
Junction-to-Ambient (PCB Mount) , D^2Pak ⑦⑧	$R_{\theta JA}$		40	°C/W

6.Electrical Characteristics @ T_J= 25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=250μA, V_{GS}=0V	100			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D=5mA,Reference to 25°C①		0.12		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=58A ④		7.2	9	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=150μA	2		4	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=100V, V_{GS}=0V			20	μA
		V_{DS}=80V, V_{GS}=0V, T_J=125°C			250	μA
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=20V			100	nA
Gate-to-Source Reverse Leakage		V_{GS}=-20V			-100	nA
Internal Gate Resistance	R_g			0.7		Ω
Forward Transconductance	g_{FS}	V_{DS}=10V, I_D=58A	140			S
Total Gate Charge	Q_g	I_D=58A, V_{DS}=50V V_{GS}=10V ④		83	120	nC
Gate-to-Source Charge	Q_{gs}			9		nC
Gate-to-Drain ("Miller") Charge	Q_{gd}			27		nC
Total Gate Charge Sync.(Q_g-Q_{gd})	Q_{sync}	I_D=58A, V_{DS}=0V, V_{GS}=10V ④		56		nC
Tum-On Delay Time	$t_{D(on)}$	V_{DD}=65V, I_D=58A R_G=2.7Ω, V_{GS}=10V ④		16		ns
Rise Time	t_r			52		ns
Turn-Off Delay Time	$t_{D(off)}$			43		ns
Fall Time	t_f			57		ns
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=50V See Fig. 5, f=1MHz		4820		pF
Output Capacitance	C_{oss}			340		pF
Reverse Transfer Capacitance	C_{rss}			170		pF
Effective Output Capacitance (Energy Related) ⑥	C_{oss}eff.(ER)	V_{GS}=0V, V_{DS}=0V to 80V ⑥ See Fig. 11		420		pF
Effective Output Capacitance (Time Related) ⑤	C_{oss}eff.(TR)	V_{GS}=0V, V_{DS}=0V to 80V ⑤		690		pF

Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			97	A
Pulsed Source Current (Body Diode) ①	I_{SM}				390	A
Diode Forward Voltage	V_{SD}	T_J=25°C, I_S=58A, V_{GS}=0V ④			1.3	V
Reverse Recovery Time	t_{rr}	T_J=25°C, V_R=85V		38	57	ns
		T_J=125°C, I_F=58A		46	69	ns
Reverse Recovery Charge	Q_{rr}	T_J=25°C, dI/dt=100A/μs ④		53	80	nC
		T_J=125°C		82	120	nC
Reverse Recovery Current	I_{RRM}	T_J=125°C		2.5		A
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Limited by T_{Jmax}, starting T_J=25°C, L=0.143mH, R_G=25Ω, I_{AS}=58A, V_{GS}=10V. Part not recommended for use above this value.

③ I_{SD} ≤ 58A, di/dt ≤ 610A/μs, V_{DD} ≤ $V_{(BR)DSS}$, TJ ≤ 175°C.

④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑤ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑥ C_{oss} eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.

⑦ R_θ is measured at TJ approximately 90°C.

7.1Typical Characterisitics

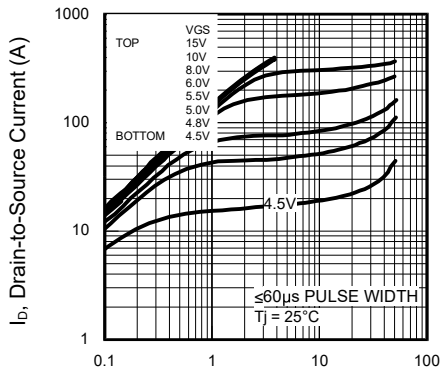


Figure 1: Typical On-Resistance vs. Gate Voltage

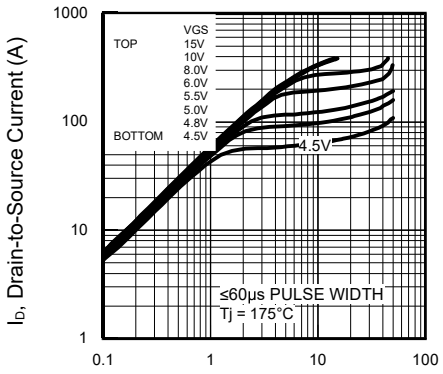


Figure 2: Typical Output Characteristics

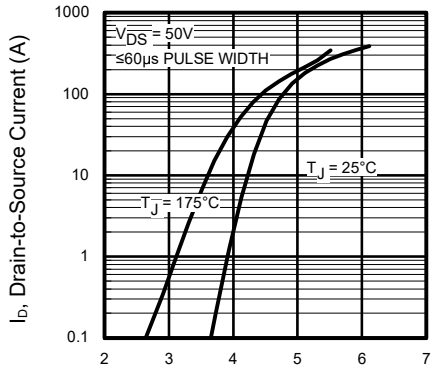


Figure 3: Typical Output Characteristics

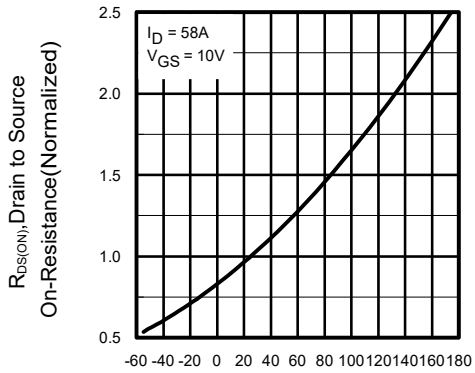


Figure 4: Normalized On-Resistance vs. Temperature

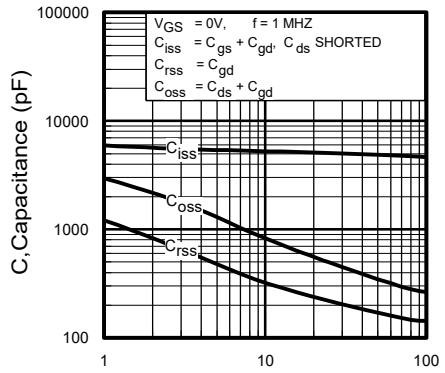


Figure 5: Typical Capacitance vs. Drain-to-Source Voltage

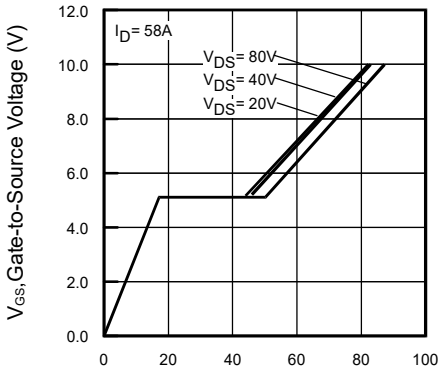
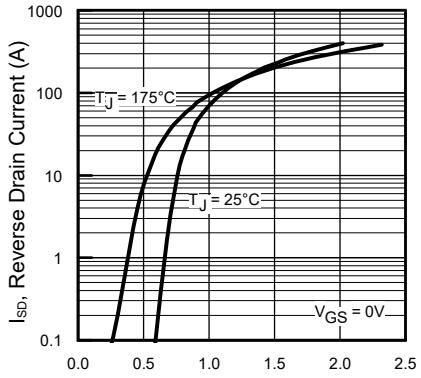


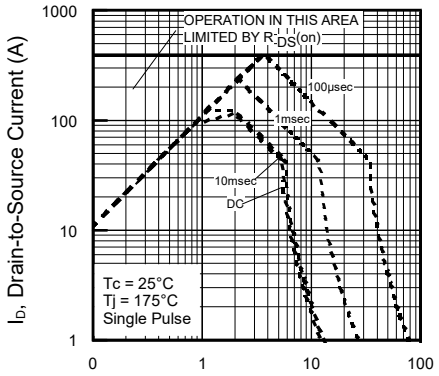
Figure 6: Typical Gate Charge vs.

7.2Typical Characterisitics



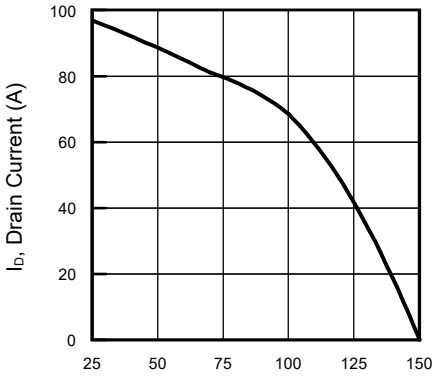
V_{SD},Source-to-Drain Voltage (V)

Figure 7: Typical Capacitance vs. Drain-to-Source Voltage



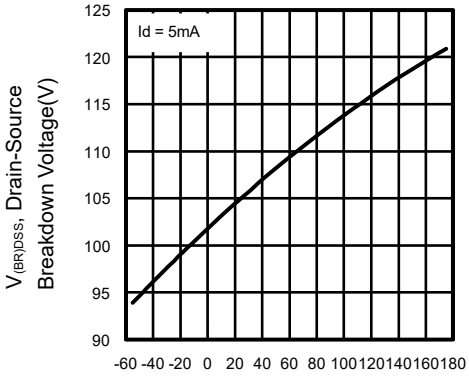
V_{DS},Drain-to-Source Voltage (V)

Figure 8: Maximum Safe Operating Area



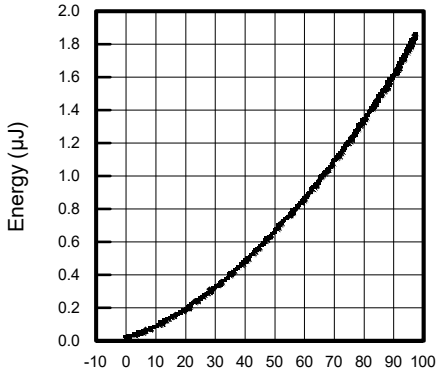
T_C,Case Temperature (°C)

Figure 9: Maximum Drain Current vs. Case Temperature



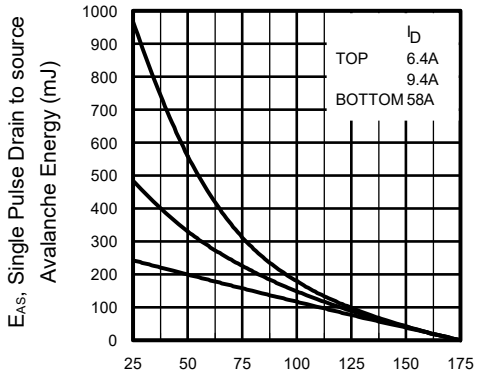
T_J,Junction Temperature (°C)

Figure 10: Drain-to-Source Breakdown Voltage



V_{DS},Drain to Source Voltage (V)

Figure 11: Typical C_{OSS} Stored Energy



Starting T_J, Junction Temperature (°C)

Figure 12: Maximum Avalanche Energy vs. DrainCurrent

7.3Typical Characterisitics

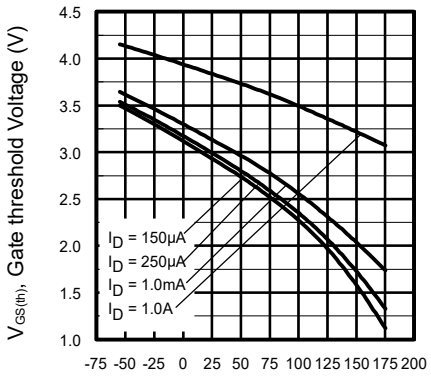


Figure 13: Threshold Voltage vs. Temperature

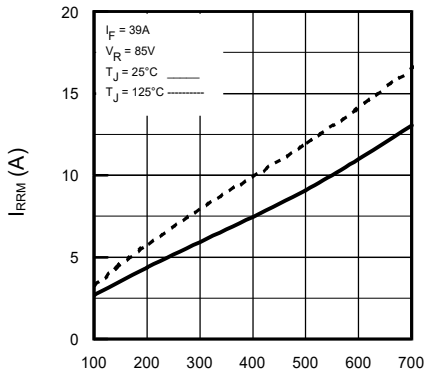


Figure 14: Typical Recovery Current vs. dif/dt

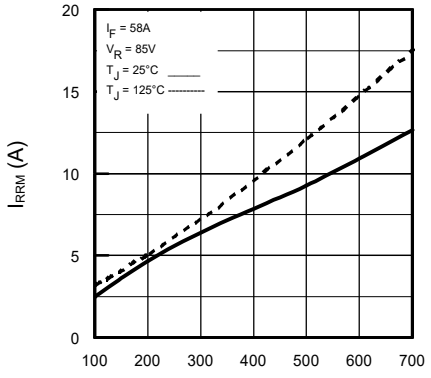


Figure 15: Typical Recovery Current vs. dif/dt

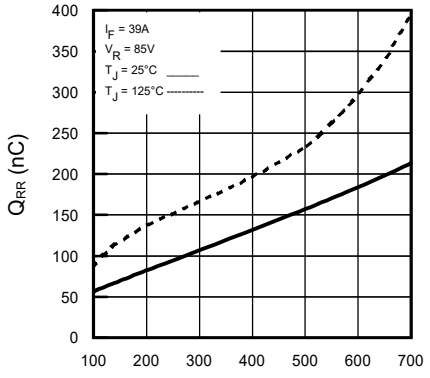


Figure 16: Typical Stored Charge vs. dif/dt

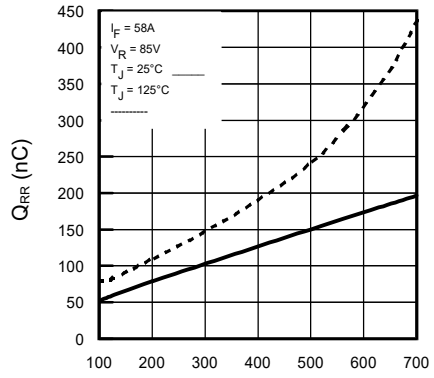


Figure 17: Typical Stored Charge vs. di_f/dt

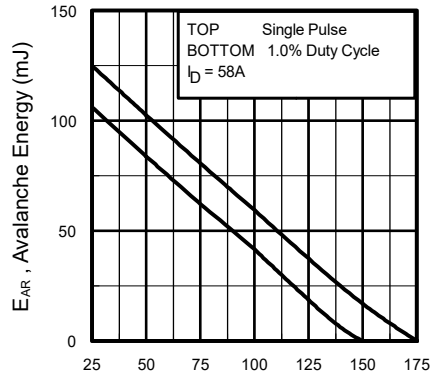


Figure 18: Maximum Avalanche Energy vs. Temperature

7.4Typical Characterisitics

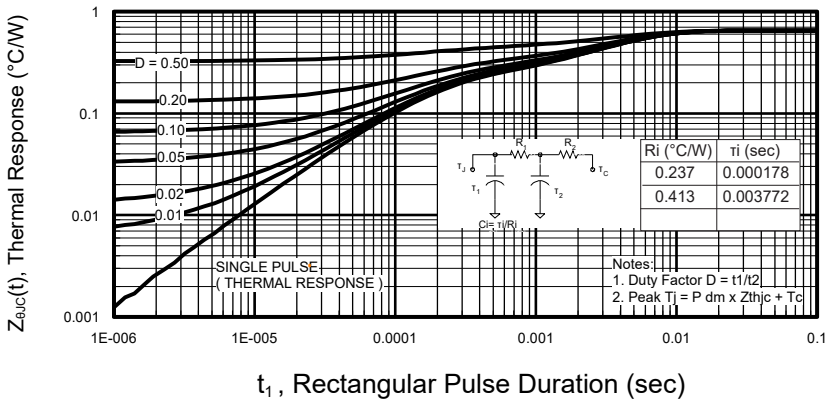


Figure 19: Maximum Effective Transient Thermal Impedance, Junction-to-Case

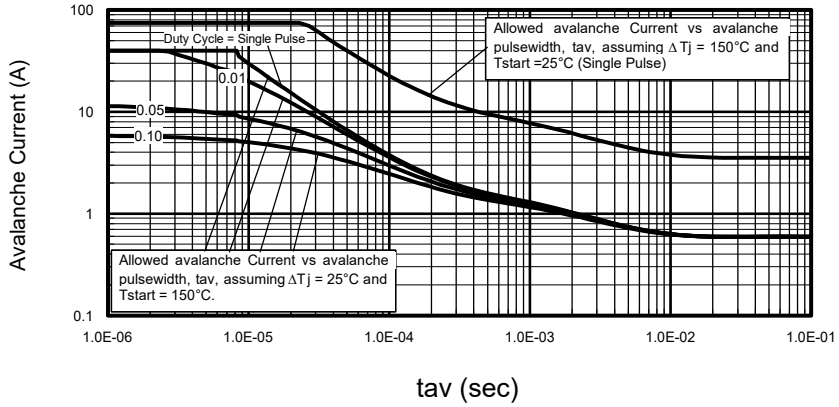


Figure 20: Typical Avalanche Current vs.Pulse width

Notes on Repetitive Avalanche Curves , Figures 18, 20:

1.Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}.

This is validated for every part type.

2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.

3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.

4. $P_{D\ (ave)}$ = Average power dissipation per single avalanche pulse.

5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).

6. I_{av} = Allowable avalanche current.

7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 18, 20).

t_{av} = Average time in avalanche.

D = Duty cycle in avalanche = t_{av} ·f

$Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figure 19)

P_D (ave) = 1/2 (1.3·BV·I_{av}) = ΔT/ Z_{thJC}

I_{av} = 2ΔT/ [1.3·BV·Zth]

$E_{AS\ (AR)}$ = P_D (ave)·t_{av}

7.5Typical Characterisitics

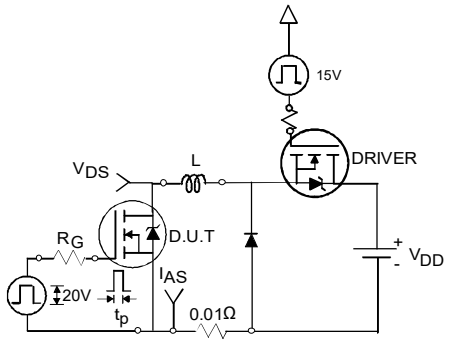


Figure 21a: Switching Time Test Circuit

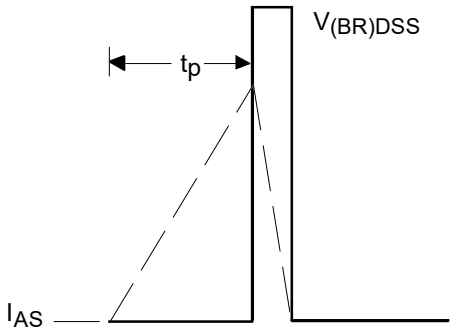


Figure 21b: Switching Time Waveforms

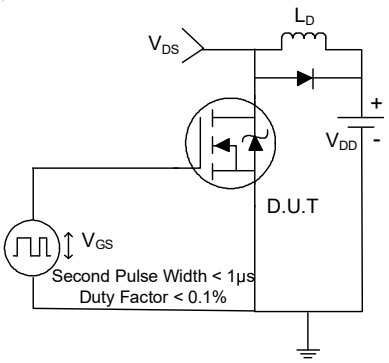


Figure 22a: Unclamped Inductive Test Circuit

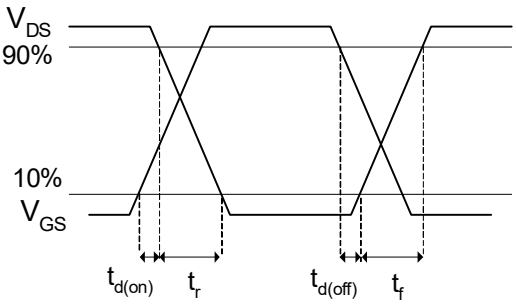


Figure 22b: Unclamped Inductive Waveforms

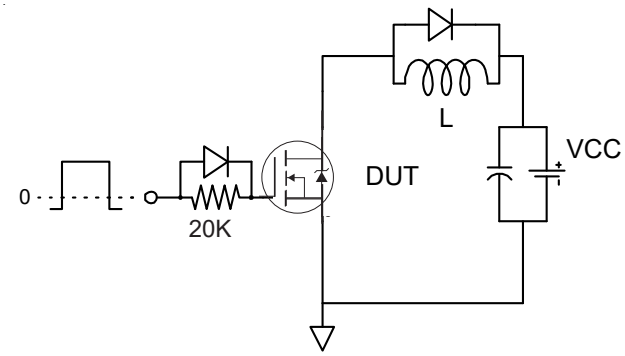


Figure 23a: Basic Gate Charge Waveform

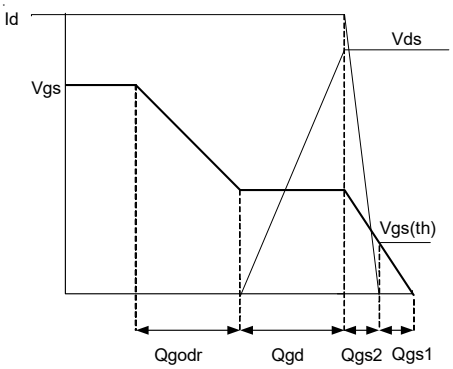
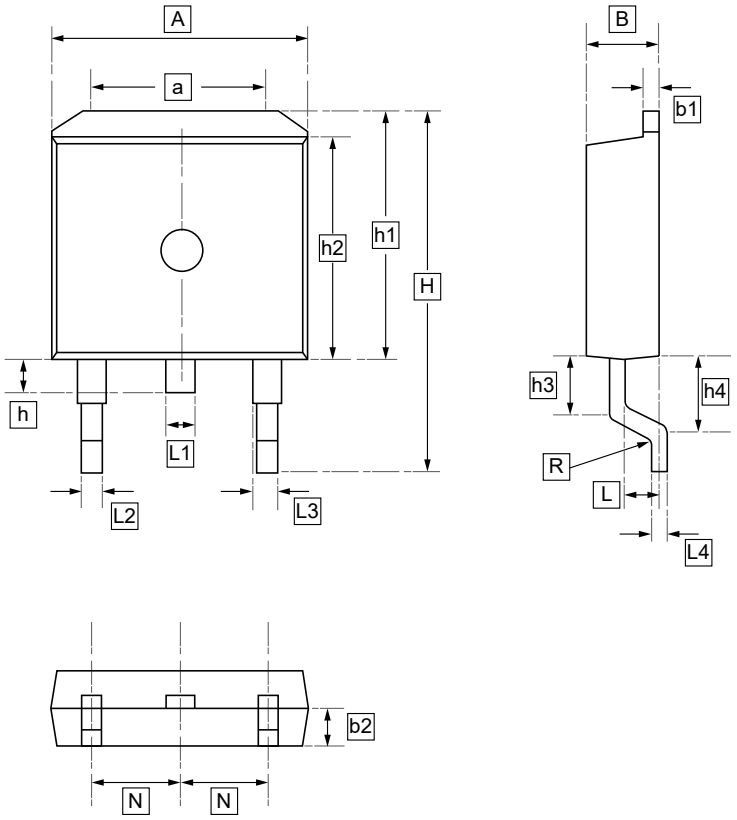


Figure 23b: Gate Charge Test Circuit

8.TO-263 Package Outline Dimensions

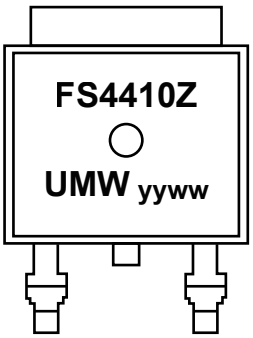


DIMENSIONS (mm are the original dimensions)

Symbol	A	a	B	b1	b2	H	h	h1	h2	h3	h4	L	L1	L2	L3
Min	9.6	7.2	4.3	1.25	2.2	15.2	1.34	10.3	9.1	1.34	2.5	2.2	1.2	0.7	1.2
Max	10.0	7.6	4.7	1.35	2.6	15.8	1.74	10.7	9.3	1.74	2.9	2.6	1.4	0.9	1.4

Symbol	L4	N	R
Min	0.4	2.4	0.45
Max	0.6	2.5	0.55

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRFS4410Z	TO-263	800	Tape and reel

10.Disclaimer

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