UMW IRLZ34NSTRL

55V N-Channel MOSFET

1.Description

Fifth Generation from International Rectifier utilize advanced processing techniques to achieve the lowest possibleon-resistance persilicon area.

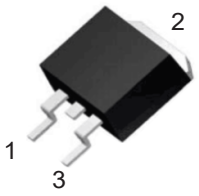
2.Features

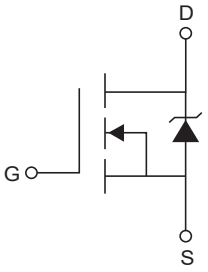
- $V_{DS\ (V)}$=55V
- I_D=16A
- $R_{DS(ON)}$<35mΩ(V_{GS}=10V)

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-263





4.Absolute Maximum Ratings

Parameter		Symbol	Rating	Units
Continuous Drain Current, V_{GS}=10V ⑤	T_C=25°C	I_D	30	A
Continuous Drain Current, V_{GS}=10V ⑤	T_C=100°C		21	A
Pulsed Drain Current ①⑤		I_{DM}	110	A
Power Dissipation	T_C=25°C	P_D	68	W
Linear Derating Factor			0.45	W/°C
Gate-to-Source Voltage		V_{GS}	±16	V
Single Pulse Avalanche Energy ②⑤		E_{AS}	110	mJ
Avalanche Current ①		I_{AR}	16	A
Repetitive Avalanche Energy ①		E_{AR}	6.8	mJ
Peak Diode Recovery dv/dt ③⑤		dv/dt	5	V/ns
Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C
Soldering Temperature, for 10 seconds			300 (1.6mm from case)	°C

5.Thermal resistance rating

Parameter	Symbol	Typ	Max	Units
Junction-to-Case	$R_{\theta JC}$		2.2	°C/W
Junction-to-Ambient (PCB Mounted.steady-state) **	$R_{\theta JA}$		40	°C/W

6.Electrical Characteristics @ T_J= 25°C (unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=250μA, V_{GS}=0V	55			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D=1mA,Reference to 25°C		0.065		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=16A ④			35	mΩ
		V_{GS}=5V, I_D=16A ④			46	mΩ
		V_{GS}=4V, I_D=14A ④			60	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1		2	V
Forward Transconductance	g_{FS}	V_{DS}=25V, I_D=16A ⑤	11			S
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=55V, V_{GS}=0V			25	μA
		V_{DS}=44V,V_{GS}=0V,T_J=150°C			250	μA
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=16V			100	nA
Gate-to-Source Reverse Leakage		V_{GS}=-16V			-100	nA
Total Gate Charge	Q_g	I_D=16A			25	nC
Gate-to-Source Charge	Q_{gs}	V_{DS}=44V, V_{GS}=5V			5.2	nC
Gate-to-Drain ("Miller") Charge	Q_{gd}	See Fig.6 and 13 ④⑤			14	nC
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=28V		8.9		ns
Rise Time	t_r	I_D=16A		100		ns
Turn-Off Delay Time	$t_{D(off)}$	R_G=6.5Ω,V_{GS}=5V		21		ns
Fall Time	t_f	R_D=1.8Ω, See Fig. 10 ④⑤		29		ns
Internal SOurce Inductance	L_S	Between lead, and center of die contact		7.5		nH
Input Capacitance	C_{iss}	V_{GS}=0V		880		pF
Output Capacitance	C_{oss}	V_{DS}=25V		220		pF
Reverse Transfer Capacitance	C_{rss}	f=1.0MHz, See Fig. 5 ⑤		94		pF

Diode Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			30	A
Pulsed Source Current (Body Diode) ①	I_{SM}				110	A
Diode Forward Voltage	V_{SD}	T_J=25°C,I_S=16A,V_{GS}=0V④			1.3	V
Reverse Recovery Time	t_{rr}	T_J=25°C,I_F=16A di/dt=-100A/μs ④⑤		76	110	ns
Reverse Recovery Charge	Q_{rr}			190	290	nC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max.junction temperature.(See fig.11)

② V_{DD}=25V, starting T_J= 25°C, L=610μH, R_G=25Ω, I_{AS}=16A.(See Figure 12)

③ I_{SD}≤ 16A, didt ≤270A/μs, V_{DD}≤ $V_{(BR)DSS}$,T_J≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ Uses IRLZ34N data and test conditions.

7.1Typical Characterisitics

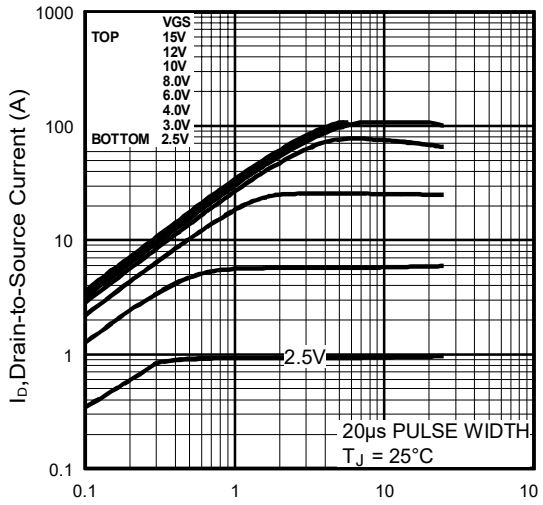


Figure 1: Typical Output Characteristics

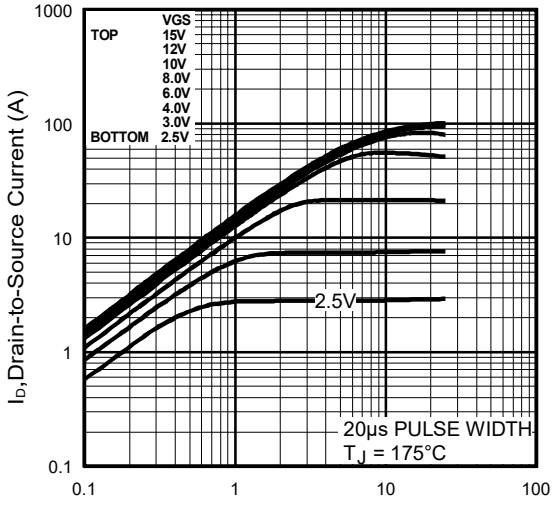


Figure 2: Typical Output Characteristics

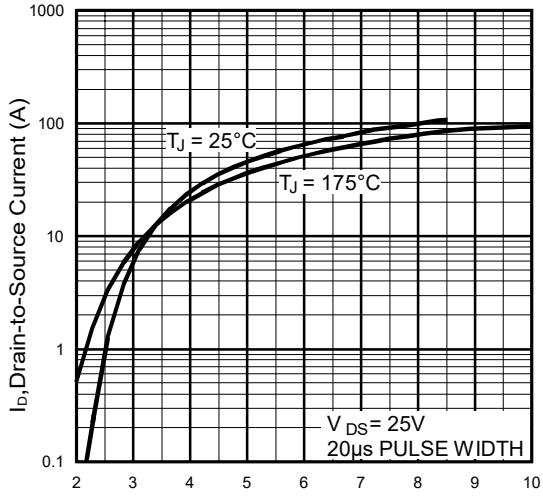


Figure 3: Typical Transfer Characteristics

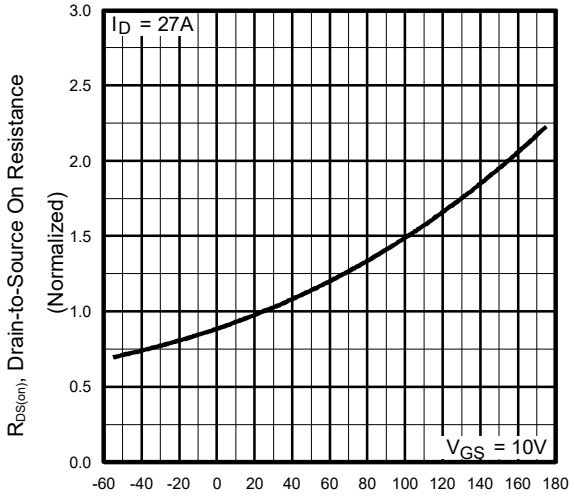


Figure 4: Nomalized On-ResistanceVs. Temperature

7.2Typical Characterisitics

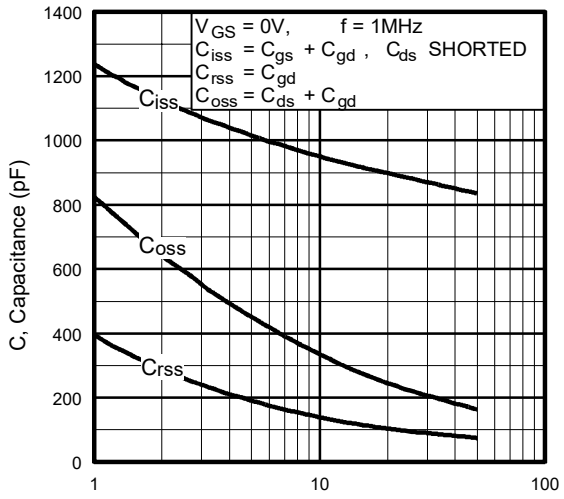


Figure 5: Typical Capacitance Vs. Drain-to-Source Voltage

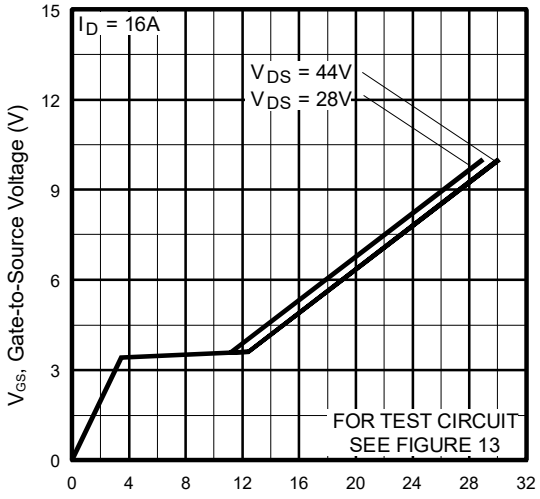


Figure 6: Typical Gate Charge Vs. Gate-to-Source Voltage

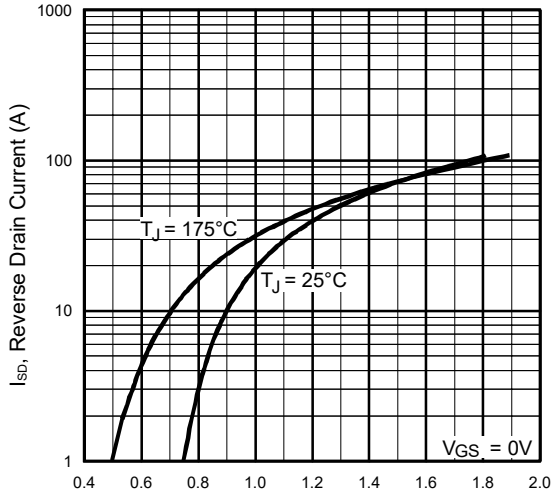


Figure 7: Typical Source-Drain Diode Forward Voltage

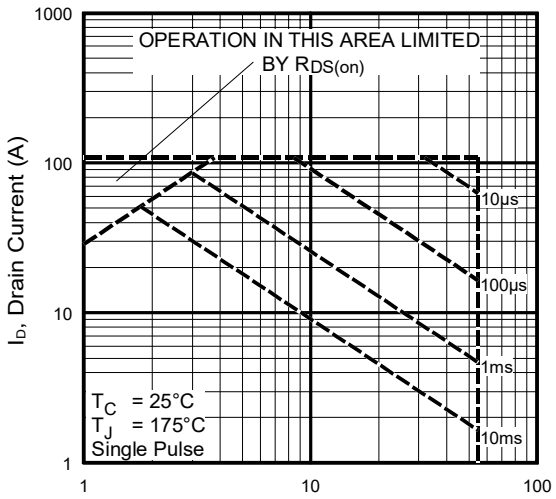


Figure 8: Maximum Safe Operating Area

7.3Typical Characterisitics

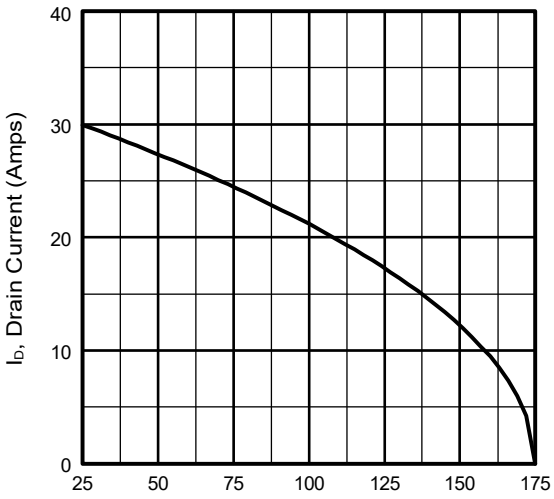


Figure 9: Maximum Drain Current Vs. Case Temperature

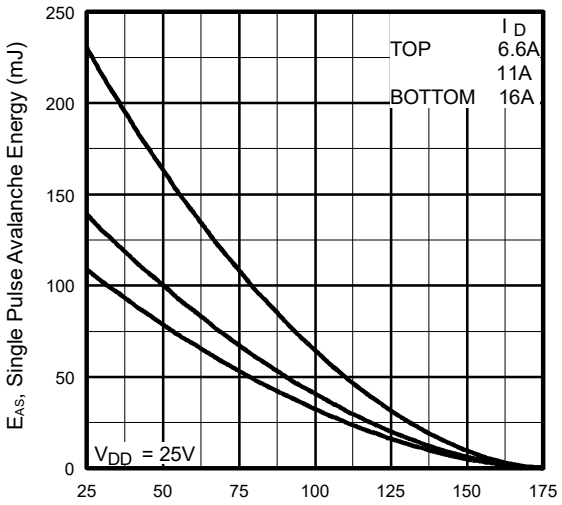


Figure 10: Maximum Avalanche Energy Vs. Drain Current

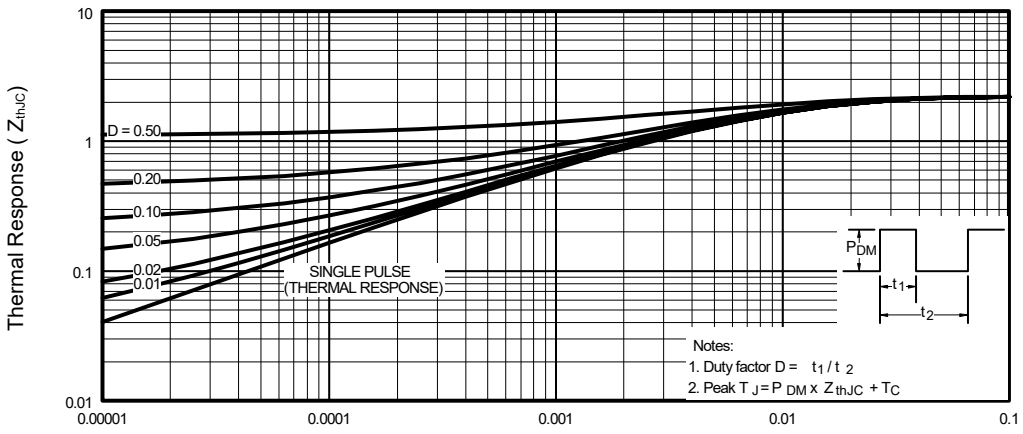


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

7.4Typical Characterisitics

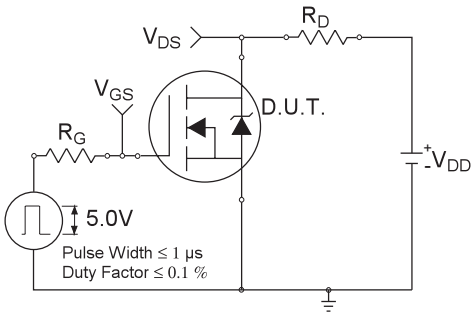


Figure 12a: Switching Time Test Circuit

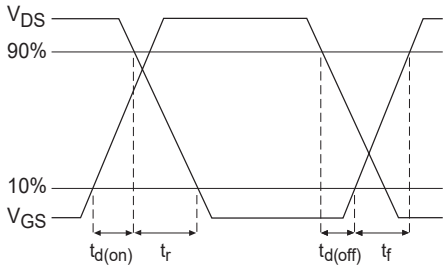


Figure 12b: Switching Time waveforms

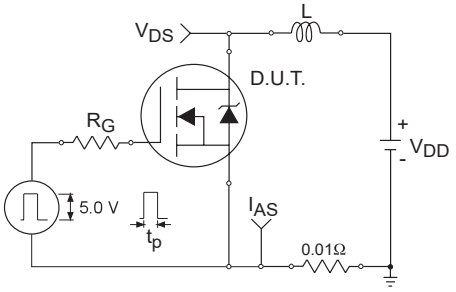


Figure 13a: Unclamped Inductive Test Circuit

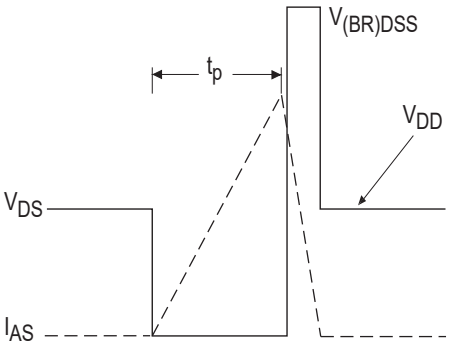


Figure 13b: Unclamped Inductive waveforms

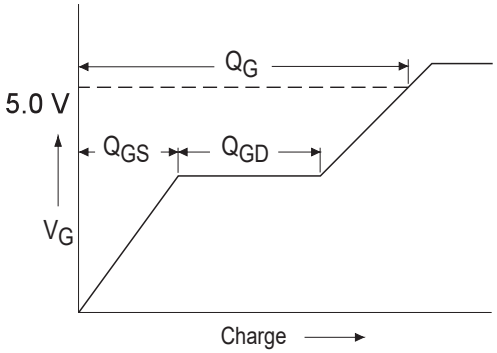


Figure 14a: Basic Gate Charge waveform

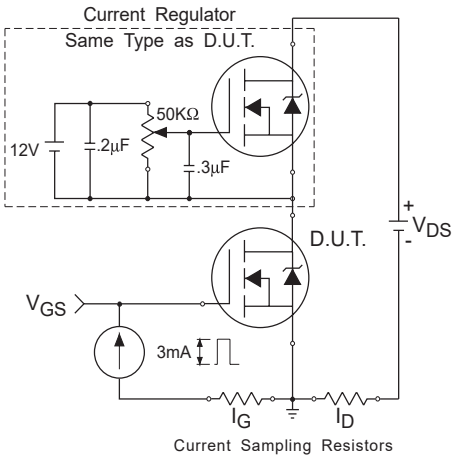
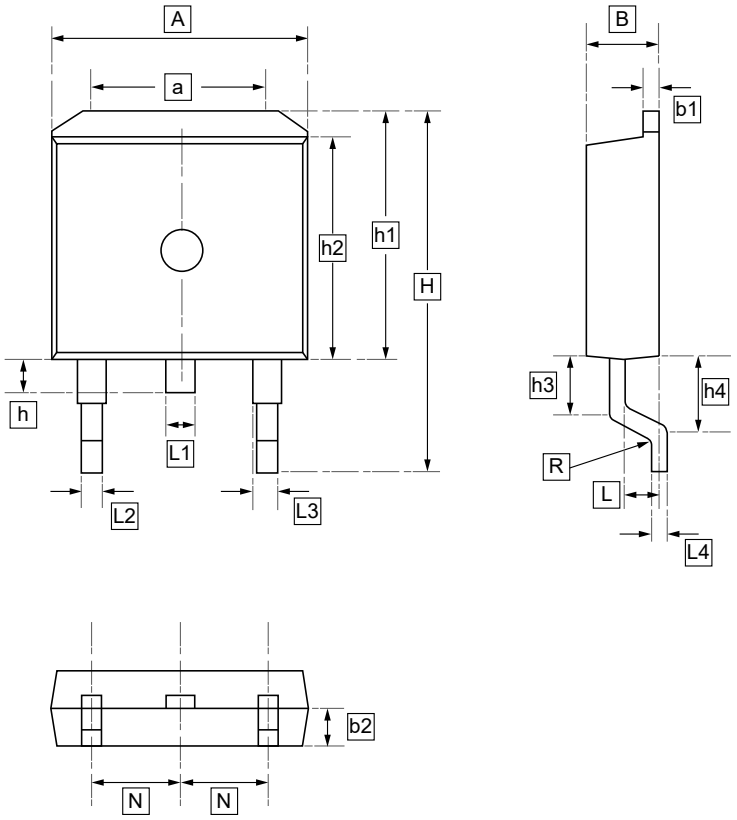


Figure 14b: Gate Charge Test Circuit

8.TO-263 Package Outline Dimensions

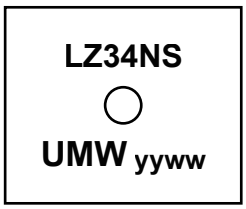


DIMENSIONS (mm are the original dimensions)

Symbol	A	a	B	b1	b2	H	h	h1	h2	h3	h4	L	L1	L2	L3
Min	9.6	7.2	4.3	1.25	2.2	15.2	1.34	10.3	9.1	1.34	2.5	2.2	1.2	0.7	1.2
Max	10.0	7.6	4.7	1.35	2.6	15.8	1.74	10.7	9.3	1.74	2.9	2.6	1.4	0.9	1.4

Symbol	L4	N	R
Min	0.4	2.4	0.45
Max	0.6	2.5	0.55

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRLZ34NSTRL	TO-263	800	Tape and reel

10.Disclaimer

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