UMW NTD4804NT4G

30V N-Channel MOSFET

1.Description

- Low $R_{DS(ON)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These Devices are Pb−Free and are RoHS Compliant
- CPU Power Delivery
- DC−DC Converters
- Low Side Switching

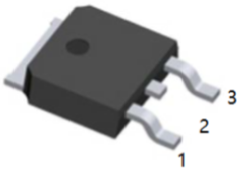
2.Features

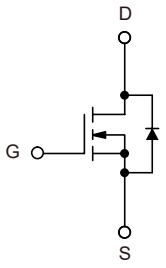
- V_{DS}(V)=30V
- I_D=117A (V_{GS}=10V)
- $R_{DS(ON)}$<4mΩ (V_{GS}=10V)
- $R_{DS(ON)}$<5.5mΩ(V_{GS}=4.5V)

3.Pinning information

Pin	Symbol	Description
1	G	GATE
2	D	DRAIN
3	S	SOURCE

TO-252(DPAK)
top view





4.Absolute Maximum Ratings T_J= 25°C

Parameter			Symbol	Value	Units
Drain−to−Source Voltage			V_{DSS}	30	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current ($R_{\theta JA}$) (Note 1)	Steady State	T_A=25°C	I_D	19.6	A
		T_A=85°C		15.2	A
Power Dissipation ($R_{\theta JA}$) (Note 1)		T_A=25°C	P_D	2.66	W
Continuous Drain Current ($R_{\theta JA}$) (Note 2)		T_A=25°C	I_D	14.5	A
		T_A=85°C		11	A
Power Dissipation ($R_{\theta JA}$) (Note 2)		T_A=25°C	P_D	1.43	W

Continuous Drain Current ($R_{\theta JC}$) (Note 1)	Steady State	T_C=25°C	I_D	124	A
		T_C=85°C		96	A
Power Dissipation ($R_{\theta JC}$) (Note 1)		T_C=25°C	P_D	107	W
Pulsed Drain Current	t_p=10μs	T_C=25°C	I_{DM}	230	A
Curent Limited by Package		T_A=25°C	$I_{DmaxPkg}$	45	A
Operating Junction and Storage Temperature		T_A=25°C	T_J,T_{STG}	−55 to 175	°C
Source Current (Body Diode)			I_S	78	A
Drain to Source dv/dt			dv/dt	6	V/ns
Single Pulse Drain−to−Source Avalanche Energy (V_{DD}=24 V,V_{GS}=10V,L=1mH, $I_{L(pk)}$=30A, R_G=25Ω)			E_{AS}	450	mJ
Lead Temperature for Soldering Purposes (1/8” from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

5.Thermal resist ance rating

Parameter	Symbol	Value	Units
Junction-to-Case (Drain)	$R_{\theta JC}$	1.4	°C/W
Junction-to-TAB (Drain)	$R_{\theta JC-TAB}$	3.5	°C/W
Junction-to-Ambient-Steady State (Note 1)	$R_{\theta JA}$	56.4	°C/W
Junction-to-Ambient-Steady State (Note 2)	$R_{\theta JA}$	105	°C/W

1. Surface−mounted on FR4 board using 1 in sq pad size, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

6.Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Parameter	Symbol	Conditions		Min	Typ	Max	Units
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250μA		30			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				26		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=0V	T_J=25°C			1	μA
		V_{DS}=24V	T_J=125°C			10	μA
Gate−to−Source Leakage Current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA		1.5		2.5	V
Negative Temperature Coefficient	$V_{GS(th)}/T_J$				7.6		mV/°C
Drain−to−Source On Resistance	$R_{DS(ON)}$	V_{GS}=10 to 11.5V	I_D=30A		3.4	4	mΩ
			I_D=15A		3.4		mΩ
		V_{GS}=4.5V	I_D=30A		4.7	5.5	mΩ
			I_D=15A		4.6		mΩ
Forward Transconductance	g_{FS}	V_{DS}=15V, I_D=15A			23		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=12V, f=1MHz			4490		pF
Output Capacitance	C_{oss}				952		pF
Reverse Transfer Capacitance	C_{rss}				556		pF
Total Gate Charge	$Q_{G(TOT)}$	V_{GS}=4.5V, V_{DS}=15V, I_D=30A			30	40	nC
Threshold Gate Charge	$Q_{G(TH)}$				5.5		nC
Gate-to-Source Charge	Q_{GS}				13		nC
Gate-to-Drain Charge	Q_{GD}				13		nC
Total Gate Charge	$Q_{G(TOT)}$	V_{GS}=11.5V, V_{DS}=15V, I_D=30A			73		nC

SWITCHING CHARACTERISTICS (Note 4)						
Turn-On Delay Time	$t_{D(on)}$	V_{GS}=4.5V, V_{DS}=15V I_D=15A, R_G=3Ω		18		ns
Rise Time	t_r			20		ns
Turn-Off Delay Time	$t_{D(off)}$			24		ns
Fall Time	t_f			8		ns
Turn-On Delay Time	$t_{D(on)}$	V_{GS}=11.5V, V_{DS}=15V I_D=15A, R_G=3Ω		10		ns
Rise Time	t_r			19		ns
Turn-Off Delay Time	$t_{D(off)}$			35		ns
Fall Time	t_f			5		ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
Forward Diode Voltage	V_{SD}	V_{GS}=0V I_D=30A	T_J=25°C	0.81	1.2	V
			T_J=125°C	0.72		V
Reverse Recovery Time	t_{rr}	V_{GS}=11.5V, dIs/dt=100A/μs I_S=30A		34		ns
Charge Time	t_a			19		ns
Discharge Time	t_b			15		ns
Reverse Recovery Time	Q_{rr}			30		nC
PACKAGE PARASITIC VALUES						
Source Inductance	L_S	T_A=25°C		2.49		nH
Drain inductance, DPAK	L_D			0.0164		nH
Drain Inductance, IPAK	L_D			1.88		nH
Gate Inductance	L_G			3.46		nH
Gate Resistance	R_G			0.6		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7.1Typical Characterisitics

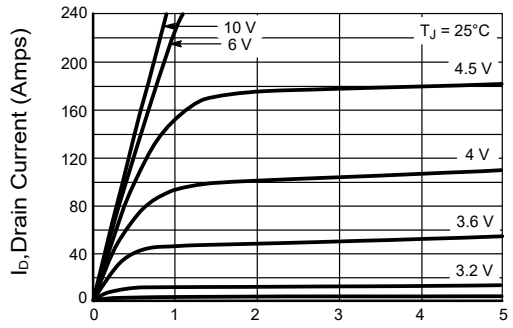


Figure 1: On−Region Characteristics

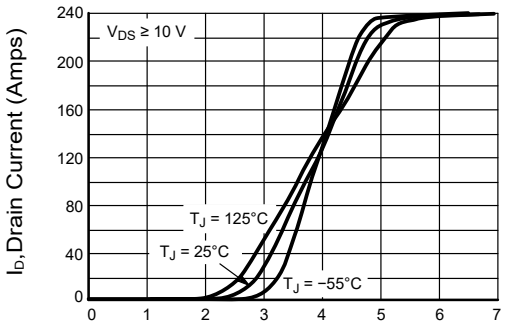


Figure 2: Transfer Characteristics

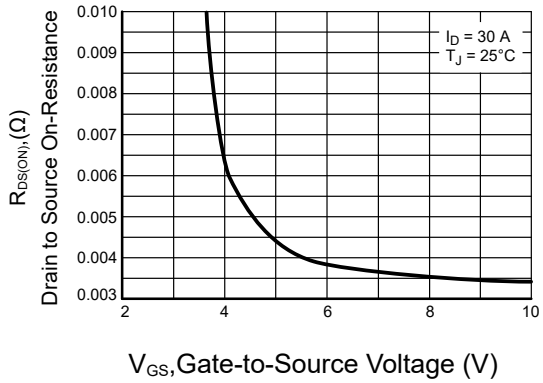


Figure 3: On−Resistance vs. Gate−to−Source Voltage

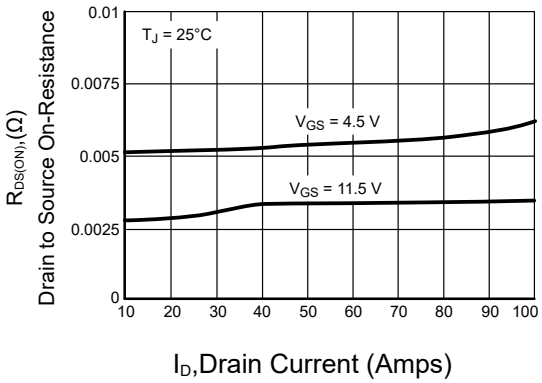


Figure 4: On−Resistance versus Drain Current and Gate Voltage

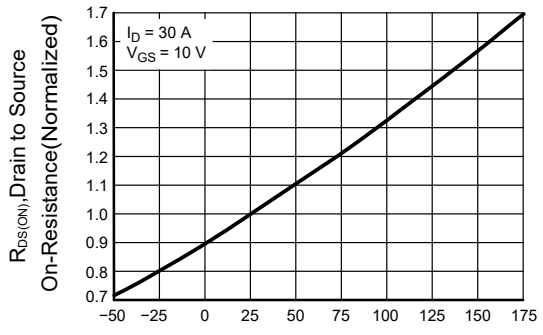


Figure 5: On−Resistance Variation with Temperature

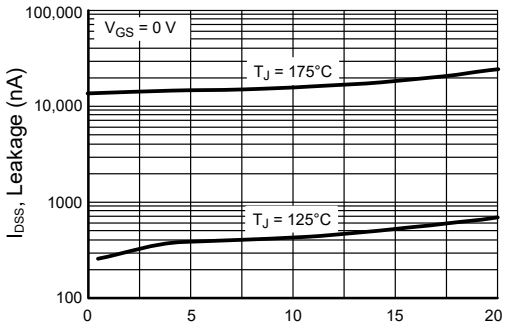
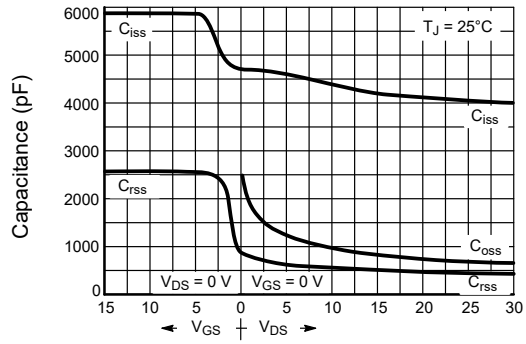


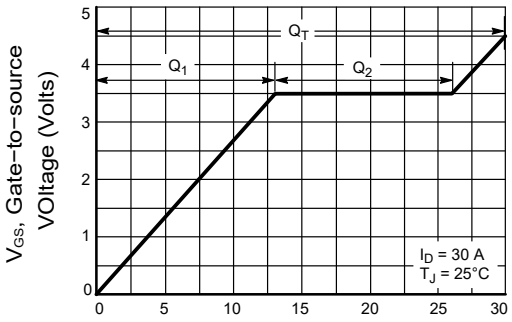
Figure 6: Drain−To−Source Leakage Current versus Voltage

7.2Typical Characterisitics



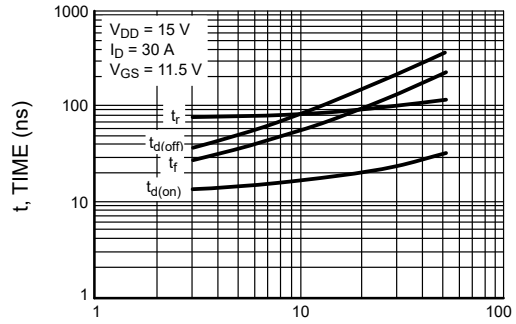
Gate−to−source Or Drain−to−source Voltage (Volts)

Figure 7: Capacitance Variation



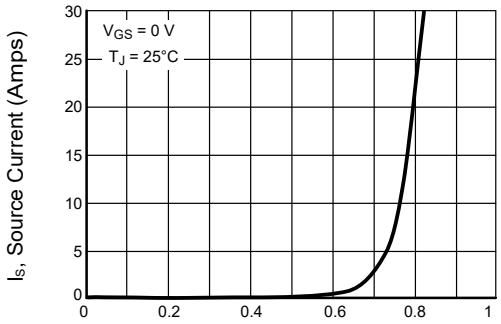
Q_G, Total Gate Charge (nC)

Figure 8: Gate−To−Source and Drain−To−Source Voltage vs. Total Charge



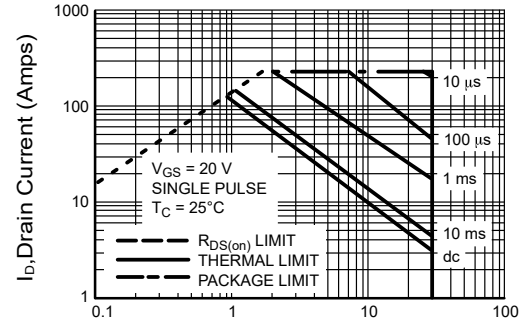
R_G, Gate Resistance (OHMS)

Figure 9: Resistive Switching Time Variation vs. Gate Resistance



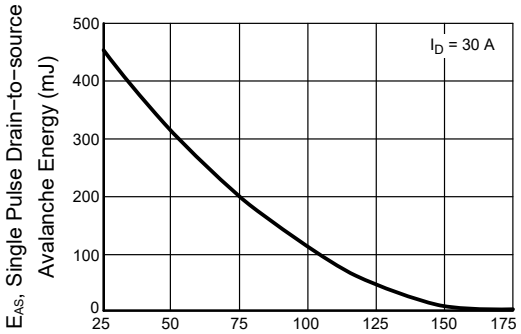
V_{SD}, Source−to−drain Voltage (VOLTS)

Figure 10: On−Resistance versus Drain Current and Gate Voltage



V_{DS}, Drain−to−source Voltage (Volts)

Figure 11: Maximum Rated Forward Biased Safe Operating Area



T_J,Junction Temperature (°C)

Figure 12: Maximum Avalanche Energy vs. Starting Junction Temperature

7.3Typical Characterisitics

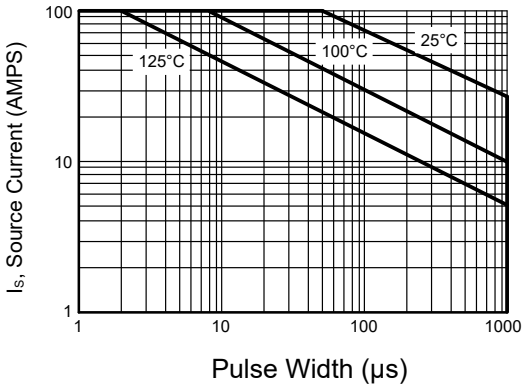


Figure 13: Avalanche Characteristics

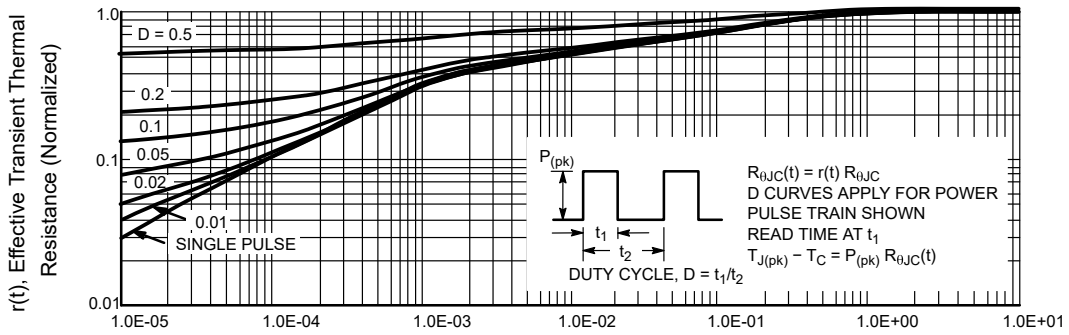
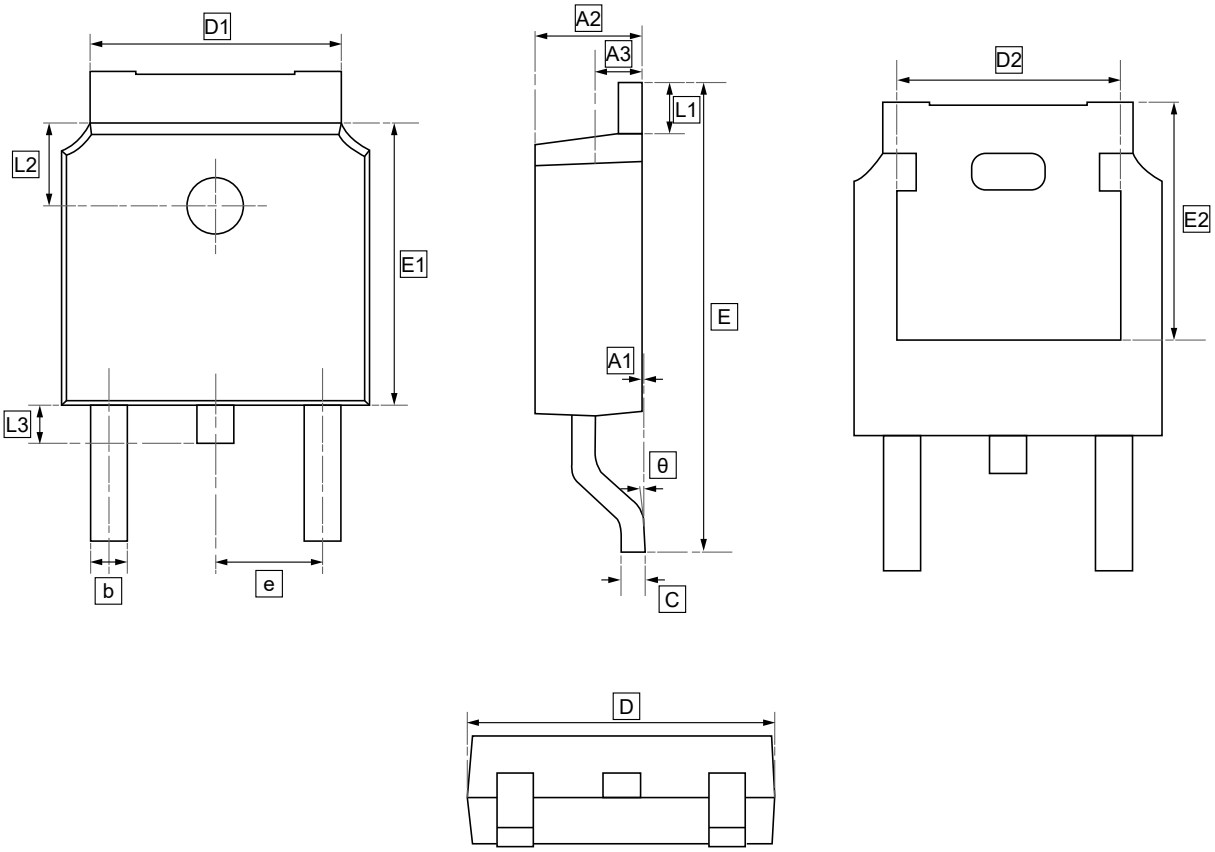


Figure 14: Diode Forward Voltage versus Current

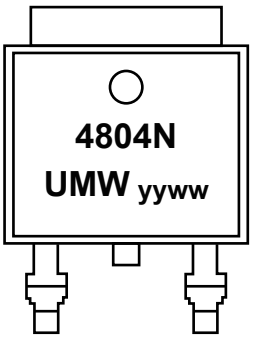
7.TO-252 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A1	A2	A3	b	c	D	D1	D2	E	E1	E2	e	L1	L2	L3	θ
Min	0.00	2.18	0.90	0.65	0.46	6.35	4.95	4.32	9.40	5.97	5.21	2.286	0.89	1.70	0.60	0.00
Max	0.13	2.39	1.10	0.85	0.61	6.73	5.46	4.90	10.41	6.22	5.38	BSC	1.27	1.90	1.00	8.00

8.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW NTD4804NT4G	TO-252	2500	Tape and reel

9.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.