UMW SI9945BDY

Dual N-Channel MOSFET

1.Features

- $V_{DS(V)}$=60V, I_D=5.3A
- $R_{DS(ON)}$<0.035Ω(V_{GS}=10V)
- $R_{DS(ON)}$<0.045Ω(V_{GS}=4.5V)

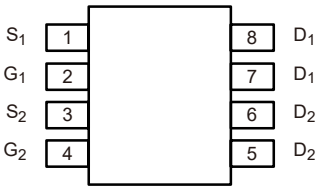
2.Applications

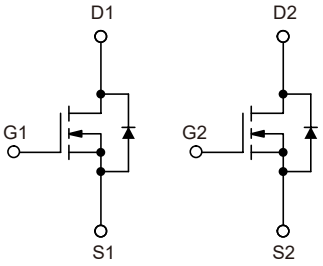
- LCD TV CCFL inverter
- Load switch

3.Pinning information

Pin	Symbol	Description
2,4	G1,G2	GATE
1,3	S1,S2	SOURCE
5,6,7,8	D1,D2	DRAIN

SOP-8





4.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current (T_J = 150 °C)	T_C=25°C	I_D	5.3	A
	T_C=70°C		4.3	
	T_A=25°C		4.3[b,c]	
	T_A=70°C		3.4[b,c]	
Pulsed Drain Current (10 μs width)		I_{DM}	20	
Continuous Source-Drain Diode Current	T_C=25°C	I_S	2.6	
	T_A=25°C		1.7[b,c]	
Avalanche current	L = 0.1 mH	I_{AS}	11	
Single-pulse avalanche energy		E_{AS}	6.1	mJ
Maximum Power Dissipation	T_C=25°C	P_D	3.1	W
	T_C=70°C		2	W
	T_A=25°C		2[b,c]	W
	T_A=70°C		1.3[b,c]	W
Operating Junction and Storage Temperature Range		T_J,T_{STG}	-55 to 150	°C

5.Thermal Resistance Rating

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [a,d]		R_{thJA}	55	62.5	°C/W
Maximum Junction-to-Foot (drain)	Steady-State	R_{thJF}	33	40	°C/W

Notes:

a. Based on T_C=25 °C

b. Surface mounted on 1" x 1" FR4 board

c. t=10s

d. Maximum under steady state conditions is 110 °C/W

6.T_J=25°C unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS}=0V, I_D=250μA	60			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D=250μA		55		mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			-6		
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1		3	V
		V_{DS}=V_{GS}, I_D=5mA		2.5		V
Gate-Source Leakage	I_{GSS}	V_{DS}=0V, V_{GS}=20V			100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V, V_{GS}=0V			1	μA
		V_{DS}=60V, V_{GS}=0V, T_J=85°C			10	
On-State Drain Current[a]	$I_{D(ON)}$	V_{DS}≥-5V, V_{GS}=10V	20			A
Drain-Source On-State Resistance[a]	$R_{DS(ON)}$	V_{GS}=10V, I_D=4.3A		0.026	0.035	Ω
		V_{GS}=4.5V, I_D=3.9A		0.035	0.045	
Forward Transconductance[a]	g_{FS}	V_{DS}=15V, I_D=4.3A		15		S
Dynamic [b]						
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, f=1MHz		665		pF
Output Capacitanc	C_{oss}			75		
Reverse Transfer Capacitance	C_{rss}			40		
Total Gate Charge	Q_g	V_{DS}=30V, V_{GS}=10V, I_D=4.3A		13	20	nC
		V_{DS}=30V, V_{GS}=4.5V, I_D=4.3A		6	9	
Gate Source Charge	Q_{gs}			2.3		
Gate Drain Charge	Q_{gd}			2.6		
Gate Resistance	R_g	f=1MHz		2		Ω
Turn-On DelayTime	$t_{D(on)}$	V_{DD} =30V, R_L=8.8Ω , I_D≌3.4A V_{GEN}=4.5V, R_g=1Ω		15	25	ns
Rise Time	t_r			65	100	
Turn-Off DelayTime	$t_{D(off)}$			15	25	
Fall Time	t_f			10	15	

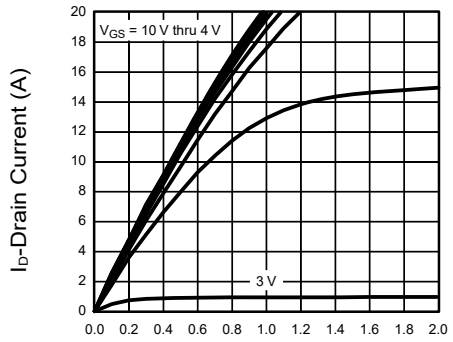
Turn-On DelayTime	$t_{D(on)}$	V_{DD} =30V, R_L=8.8Ω I_D≌3.4A, V_{GEN}=10V R_g=1Ω		10	15	ns
Rise Time	t_r			15	25	ns
Turn-Off DelayTime	$t_{D(off)}$			20	30	ns
Fall Time	t_f			10	15	ns
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C=25°C			2.6	A
Pulse Diode Forward Current	I_{SM}				20	A
Body Diode Voltage	V_{SD}	I_S=1.7A, V_{GS}=0V		0.8	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F=1.7A, dI/dt=100A/μs T_J=25°C		30	60	ns
Body Diode Reverse Recovery Charge	Q_{rr}			32	50	nC
Reverse Recovery Fall Time	t_a			25		ns
Reverse Recovery Rise Time	t_b			5		ns

Notes:

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.

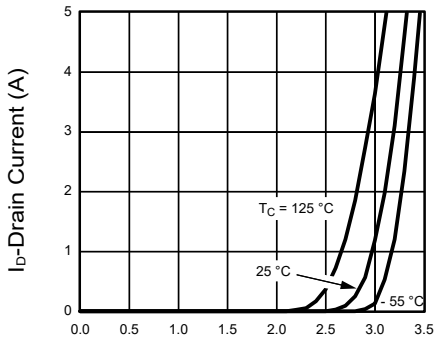
b. Guaranteed by design, not subject to production testing.

7.1Typical Characterisitics



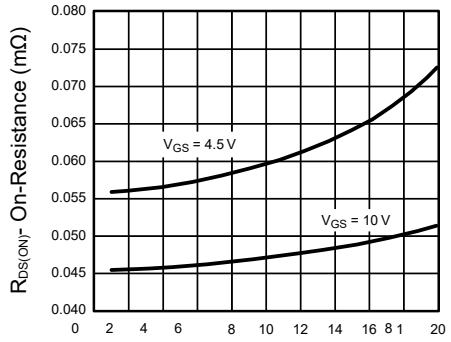
V_{DS} - Drain-to-Source Voltage (V)

Output Characteristics



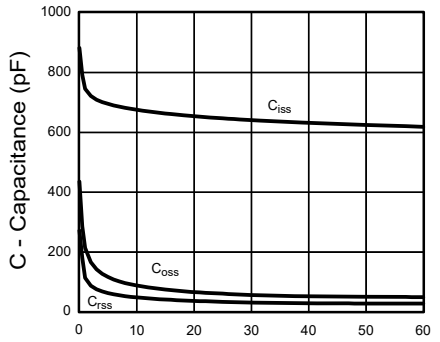
V_{GS} - Gate-to-Source Voltage (V)

Transfer Characteristics



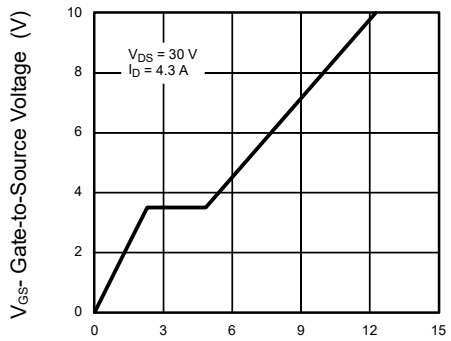
I_D-Drain Current (A)

On-Resistance vs. Drain Current and Gate Voltage



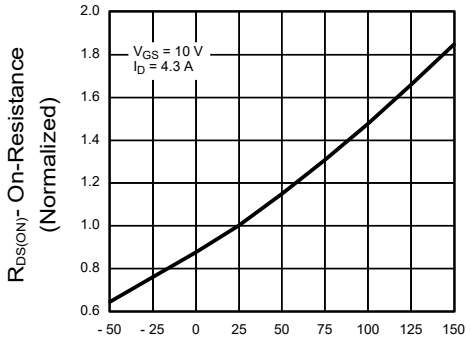
V_{DS} - Drain-to-Source Voltage (V)

Capacitance



Q_g - Total Gate Charge (nC)

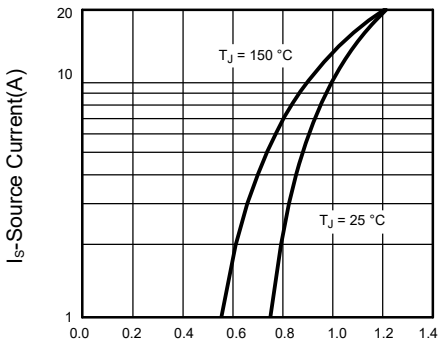
Gate Charge



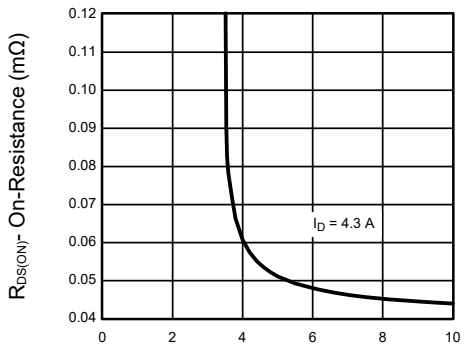
T_J - Junction Temperature (°C)

On-Resistance vs. Junction Temperature

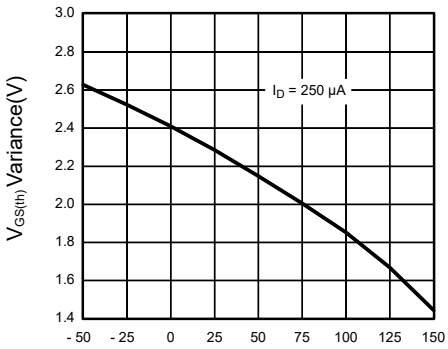
7.2Typical Characterisitics



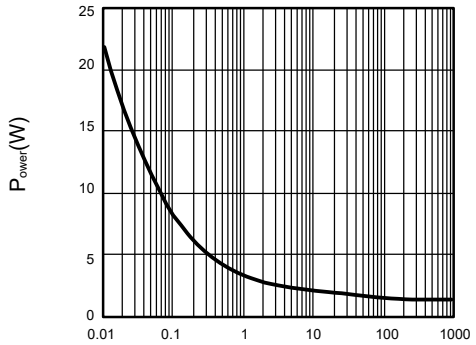
Source-Drain Diode Forward Voltage



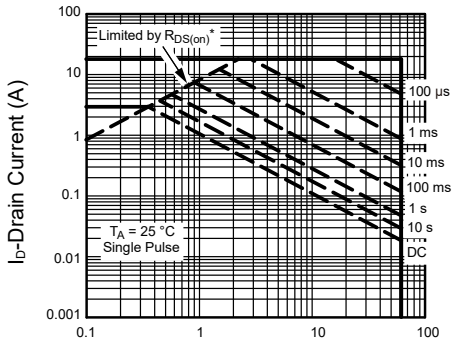
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

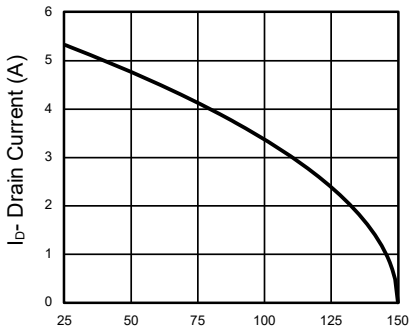


Single Pulse Power, Junction-to-Ambient

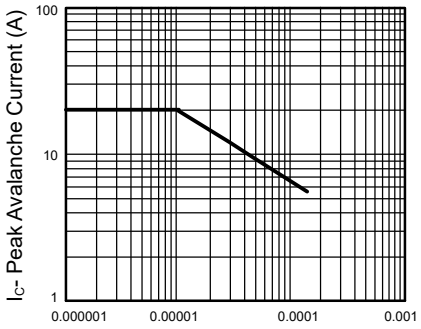


Safe Operating Area

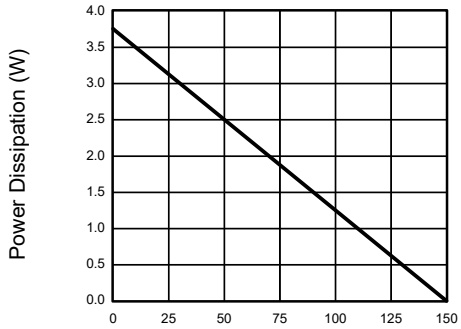
7.3Typical Characterisitics



Current Derating[a]



Single Pulse Avalanche Capability

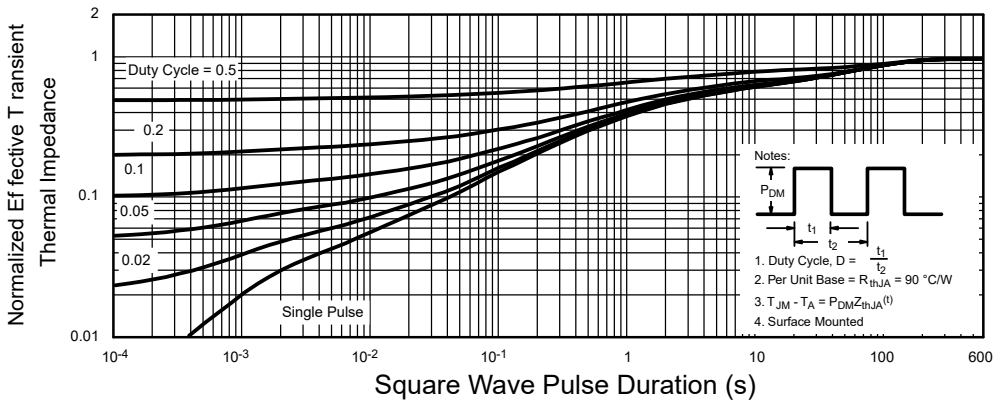


Power Derating

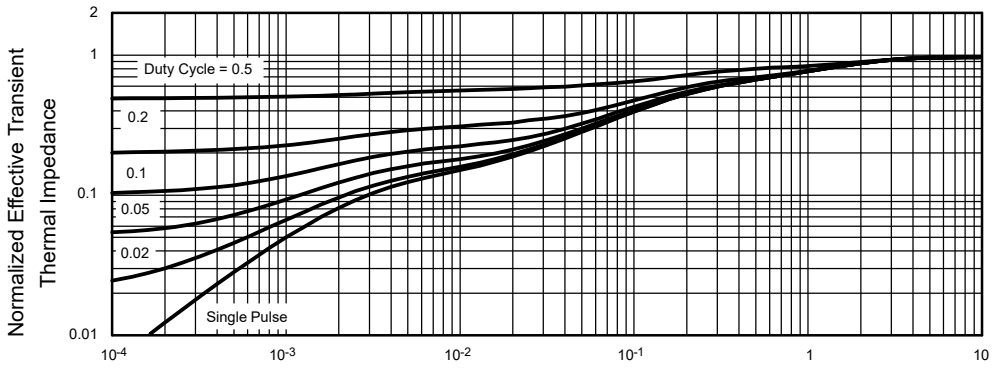
Note:

a. The power dissipation P_D is based on $T_{J(max)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

7.4Typical Characterisitics

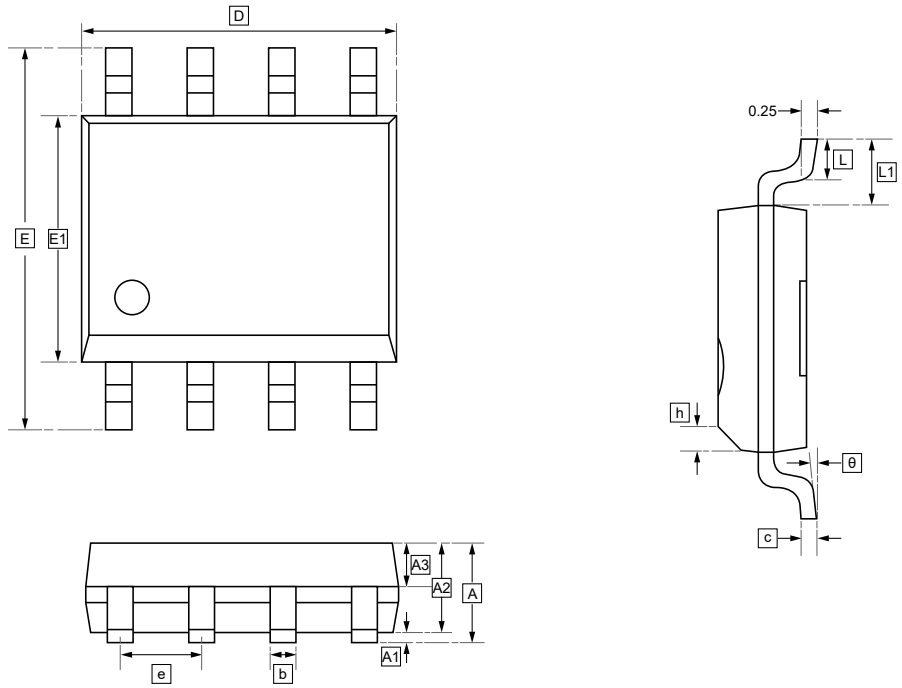


Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

8.SOP-8 Package Outline Dimensions

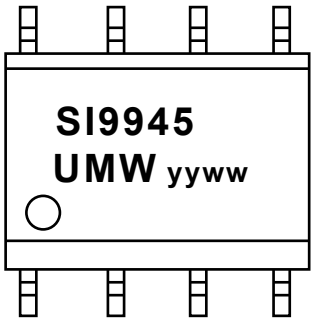


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.70	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.10	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW SI9945BDY	SOP-8	3000	Tape and reel

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