UMW TL072

General J - FET input dual operational amplifier

1.Description

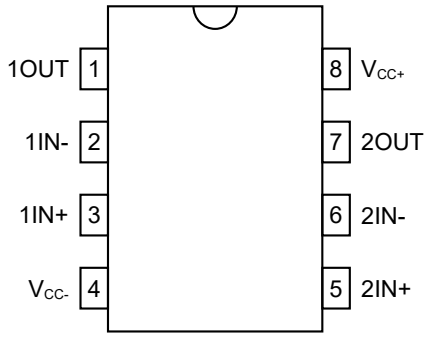
UMW TL072 is a dual operational amplifier with high-speed J-FET input, which consists of high voltage J-FET and bipolar transistor. It has high conversion rate, low input bias current and offset current, and low temperature coefficient of offset voltage. The working range is 0°C-70°C.

UMW TL072 is available in SOP8 packages.

2.Features

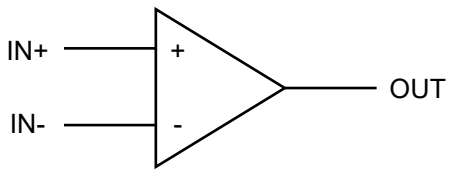
- Lower power consumption
- Wide common- mode and differential - mode input voltage range
- Low input bias current and offset current Output short - circuit current protection
- High input impedance
- High conversion rate
- High gain bandwidth product,up to 4MHz

3.Pinning Information

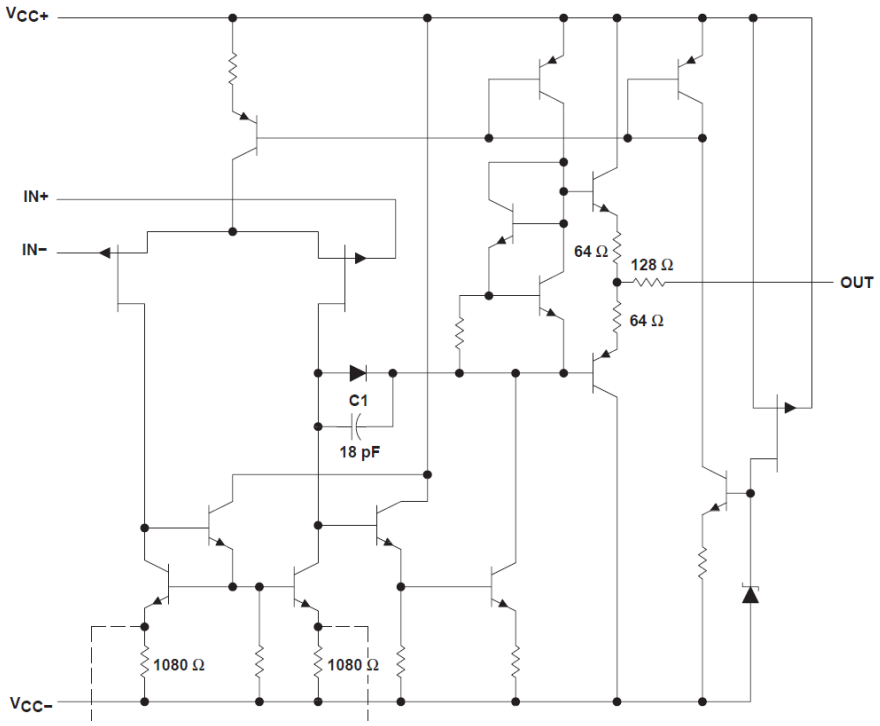


SOP-8

4.Symbol (each operational amplifier)



5.Internal Block Diagram (Each Operational Amplifier)



6.Limit Parameter

Parameter		Value	Value	Units
Power Supply Voltage		V_{CC}	±18	V
Input Voltage		V_I	±15	V
Differential Mode Input Power		V_{ID}	±30	V
Working Temperature	UMW TL072C	T_{OPER}	0 to 70	°C
	UMW TL072I		-40 to 105	°C
Storage Temperature		T_{STG}	-65 to 150	°C

7.Electrical Characteristics

V_{CC}=±15, Tamp=25°C shall be specified separately.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Offset Voltage	V_{IO}	V_O=0V		3	10	mV
Input Offset Current	I_{IO}	V_O=0V		5	100	pA
Output Bias Current	I_{IB}	V_O=0V		20	200	pA
Input Common Mode Voltage	V_{ICM}		±11	-12~15		V
Peak Output Voltage	V_{OM}	R_L=10kΩ	12	13.5		V
		R_L≥2kΩ	10	12		V
Large Signal Voltage Gain	A_{VD}	R_L≥2kΩ, V_O=±10V	25	200		V/mV
Common Mode Rejection Ratio	CMRR		70	86		dB
Power Supply Rejection Ratio	SVR	V_{CC}=±15V to ±9V, V_O=0V	70	86		dB
Static Current-per Channel	I_{CC}			1.4	2.8	mA
Conversion Rate	SR	V_I=10V	8	10		V/μs
Risetime	t_r			0.1		μs
Input Impedance	R_I			10^{12}		Ω
Rise time	t_r	V_{in}=20mV, R_L=2kΩ, C_L=100pF, unity gain		0.1		μs
Overshoot	K_{OV}	V_{in}=20mV, R_L=2kΩ, C_L=100pF, unity gain		10		%
Gain bandwidth product	GBP	V_{in}=10mV, R_L=2kΩ, C_L=100pF, F=100kHz	2.5	4		MHz
Input resistance	R_i			10^{12}		Ω
Total harmonic distortion	THD	F=1kHz, R_L=2kΩ, C_L=100pF A_V=20dB, V_O=2V_{pp}				%
Equivalent input noise voltage	e_n	R_S=100Ω, F=1KHz		15		nV/√Hz
Phase margin				45		degrees
Channel separation	V_{O1}/V_{O2}	A_V=100		120		dB

1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

8.1 Typical Characterisitics

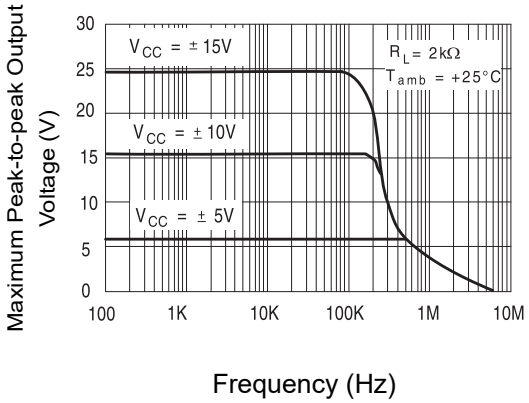


Figure 1: Maximum peak-to-peak output voltage versus frequency (R_L= 2kΩ)

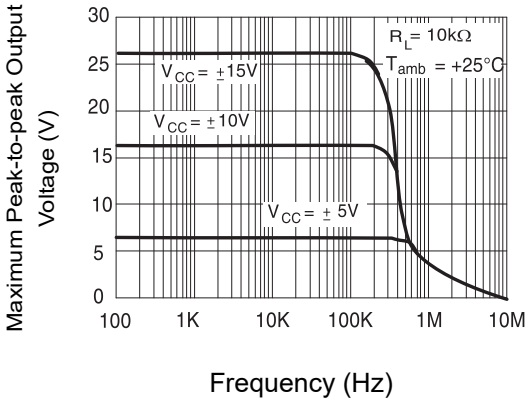


Figure 2: Maximum peak-to-peak output voltage versus frequency (R_L= 10kΩ)

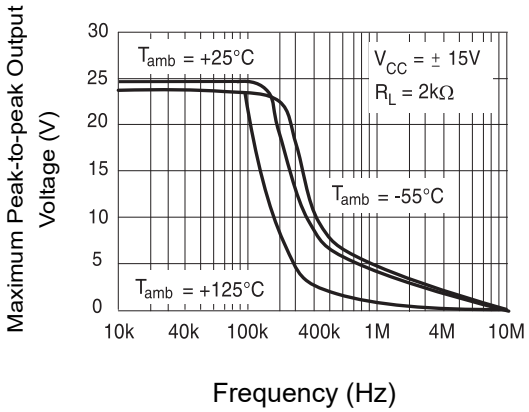


Figure 3: Maximum peak-to-peak output voltage versus frequency

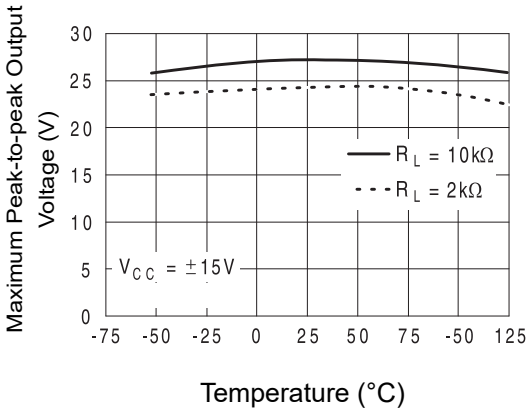


Figure 4: Maximum peak-to-peak output voltage versus free air temperature

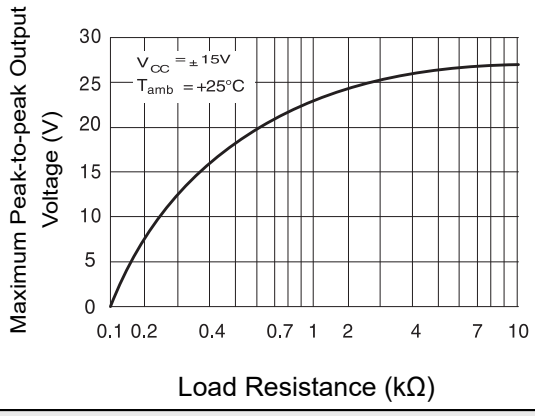


Figure 5: Maximum peak-to-peak output voltage versus load resistance

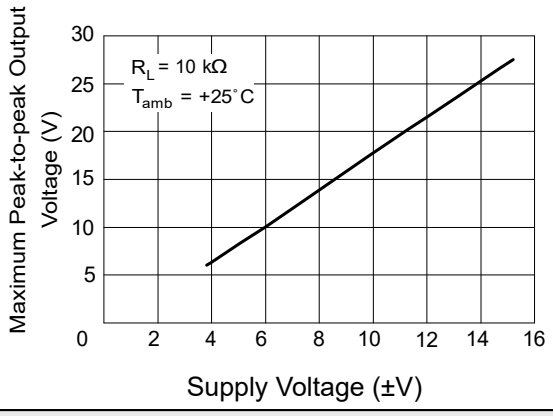


Figure 6: Maximum peak-to-peak output voltage versus supply voltage

8.2 Typical Characterisitics

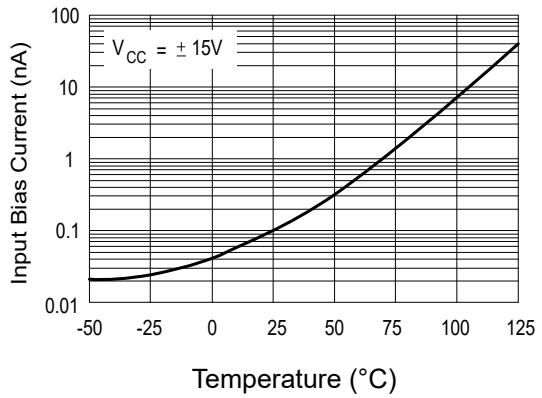


Figure 7: Input bias current versus free air temperature

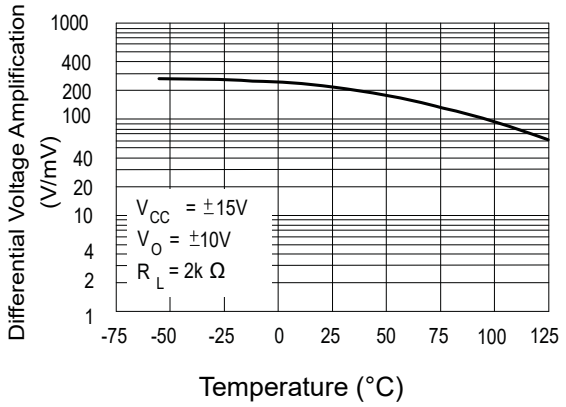


Figure 8: Large signal differential voltage amplification versus free air temp

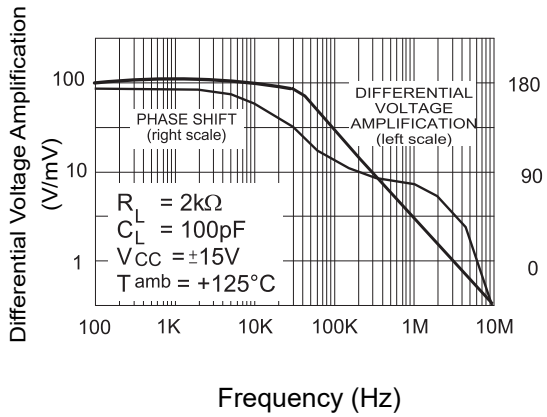


Figure 9: Large signal differential voltage amplification and phase shift versus frequency

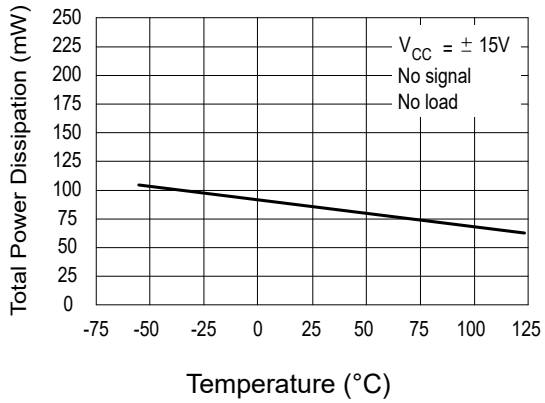


Figure 10: Total power dissipation versus free air temperature

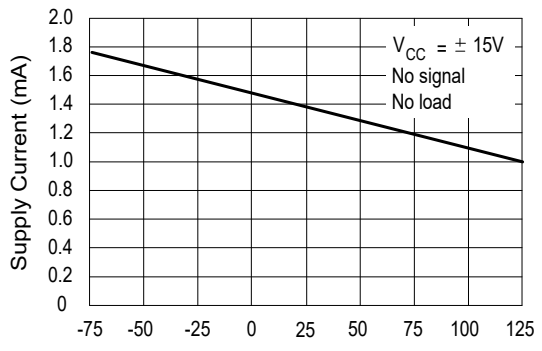


Figure 11: Supply current per amplifier versus free air temperature

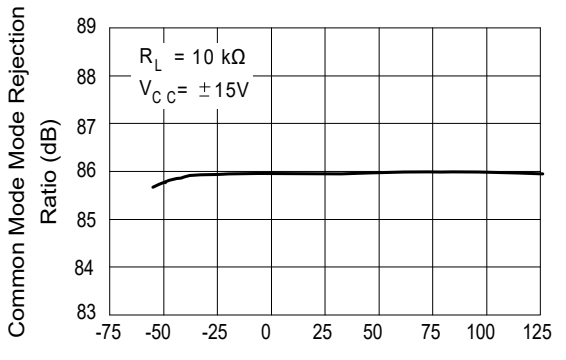


Figure 12: Common mode rejection ratio versus free air temperature

8.3 Typical Characterisitics

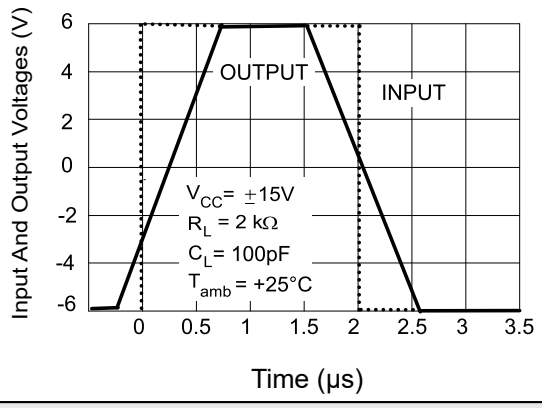


Figure 13: Voltage follower large signal pulse response

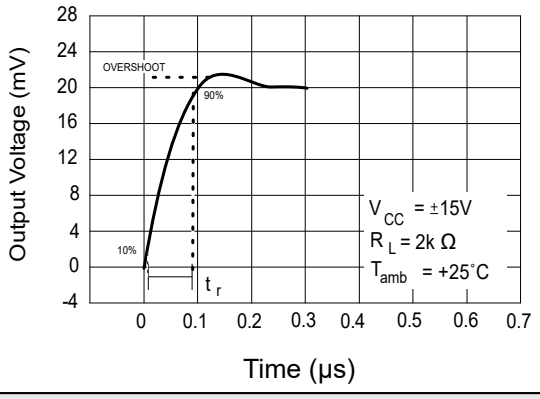


Figure 14: Output voltage versus elapsed time

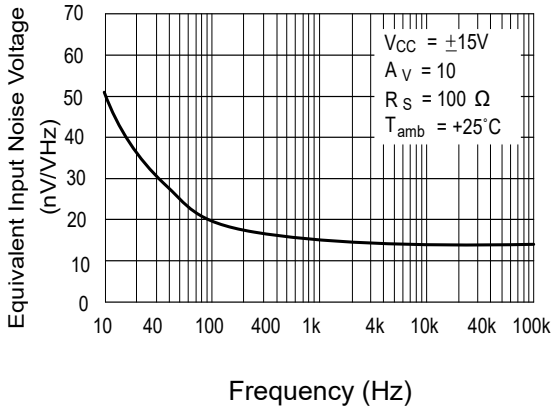


Figure 15: Equivalent input noise voltage versus frequency

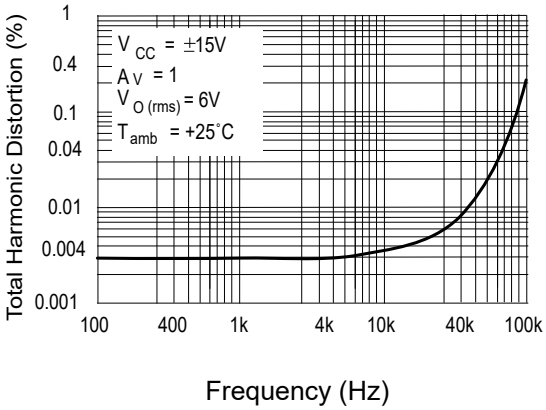


Figure 16: Total harmonic distortion versus frequency

9.Typical Application Circuit Diagram (Including One Operational Amplifier)

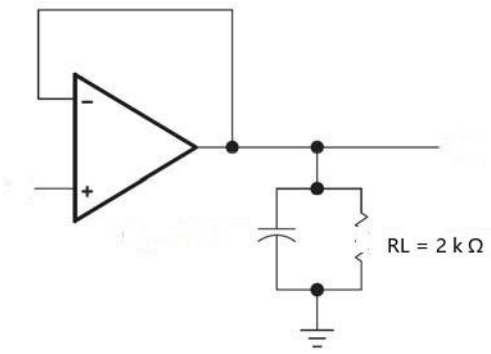


Figure 1: Unity Gain Circuit

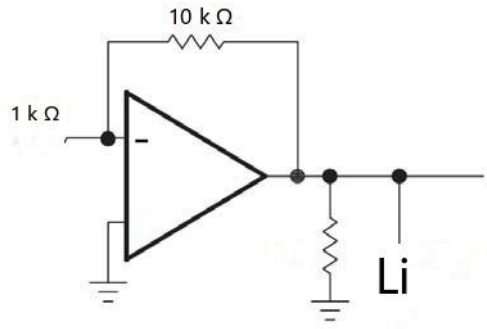


Figure 2: 10 - fold gain circuit

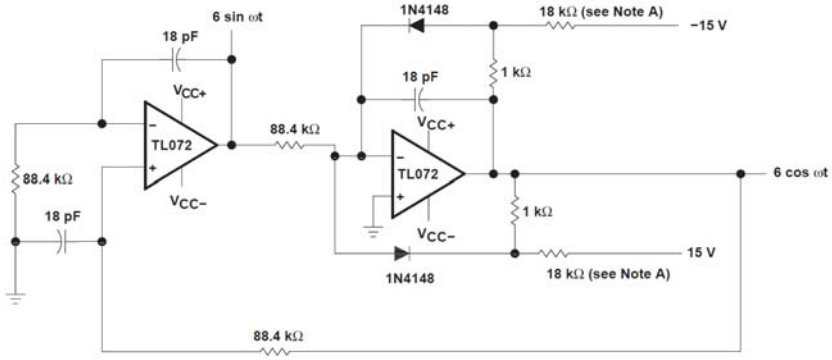


Figure 3: 100KHz oscillator

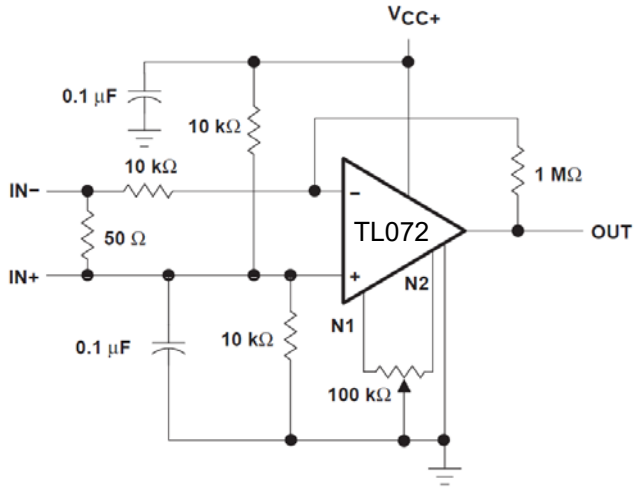


Figure 4: AC amplifier

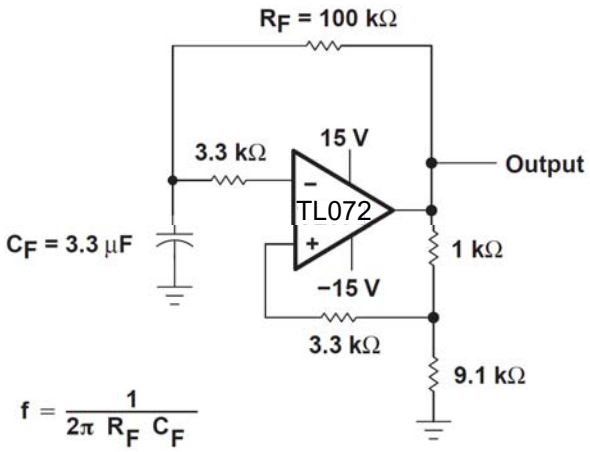
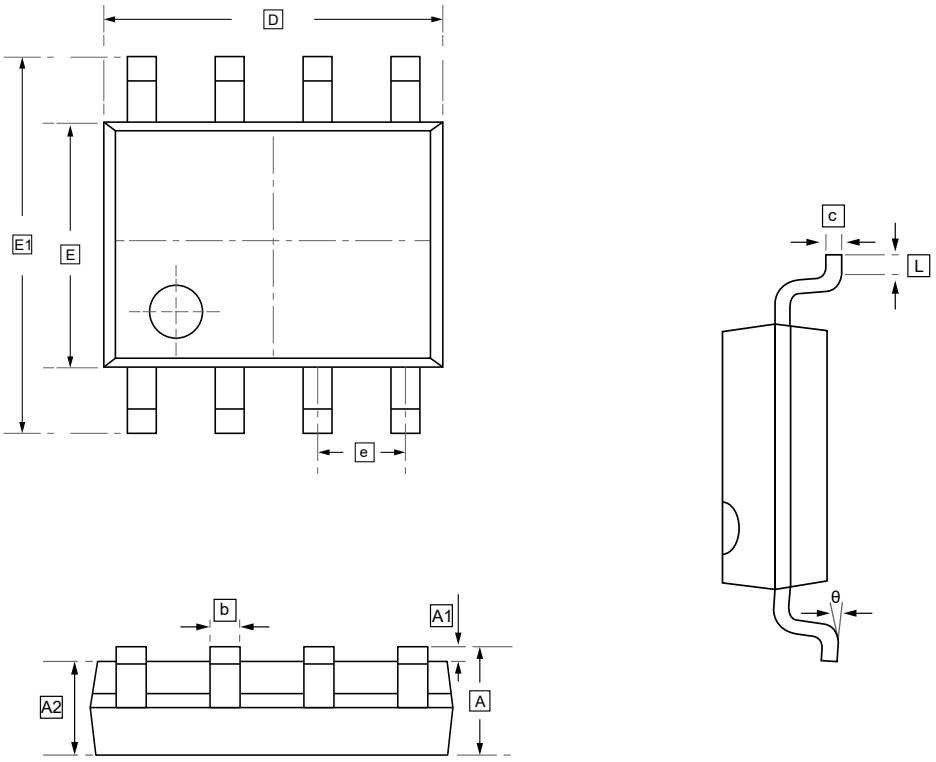


Figure 5: 0.5Hz square wave oscillator

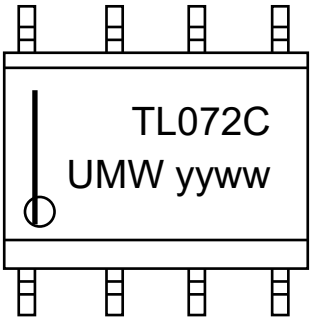
10.SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

11.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW TL072CDR	TL072C	SOP-8	2500	Tape and reel
UMW TL072IDR	TL072I	SOP-8	2500	Tape and reel

12.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.