UMW AD8531,AD8532,AD8534

Low Cost, 250 mA Output, Single-Supply Amplifiers

1.Description

The AD8531, AD8532, and AD8534 are single, dual, and quad rail-to-rail input/output single-supply amplifiers featuring 250 mA output drive current. This high output current makes these amplifiers excellent for driving either resistive or capacitive loads. AC performance is very good with 3 MHz bandwidth,5 V/μs slew rate, and low distortion. All are guaranteed to operate from a 3 V single supply as well as a 5 V supply.

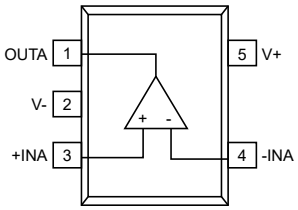
2.Features

- Single-supply operation: 2.7 V to 6 V
- High output current: ±250 mA
- Low supply current: 750 μA/amplifier
- Wide bandwidth: 3 MHz
- Slew rate: 5 V/μs
- No phase reversal
- Low input currents
- Unity gain stable
- Rail-to-rail input and output

3.Applications

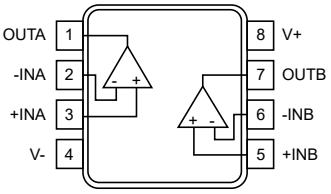
- Multimedia audio
- LCD drivers
- ASIC input or output amplifiers
- Headphone drivers

4.Pinning information



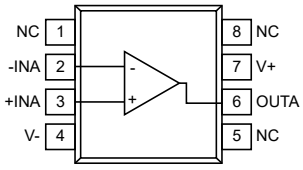
AD8531

Figure 1. 5-Lead SC70 and 5-Lead SOT-23
(KS and RT Suffixes)



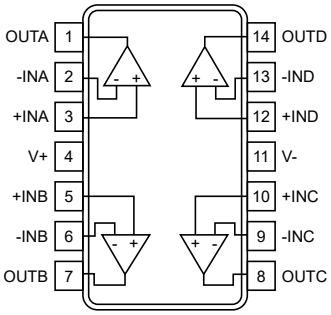
AD8532

Figure 3. 8-Lead SOP 8-Lead TSSOP
(R, RU, and RM Suffixes)



AD8531
NC=NO CONNECT

Figure 2. 8-Lead SOP
(R Suffix)



AD8534

Figure 4. 14-Lead SOP and 14-Lead TSSOP
(R and RU Suffixes)

5.Absolute Maximum Ratings

Parameter	Rating
Supply Voltage (V_S)	7V
Input Voltage	GND to V_S
Differential Input Voltage [1]	±6V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] For supplies less than 6 V, the differential input voltage is equal to ±V S.

6.1 Electrical characteristics

V_S=3V, V_{CM}=1.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Offset Voltage	V_{OS}				25	mV
		−40°C≤T_A ≤+85°C			30	mV
Input Bias Current	I_B			5	50	pA
		−40°C≤T_A ≤+85°C			60	pA
Input Offset Current	I_{OS}			1	25	pA
		−40°C≤T_A ≤+85°C			30	pA
Input Voltage Range			0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM}=0V to 3V	38	45		dB
Large Signal Voltage Gain	A_{VO}	R_L=2 kΩ, V_O=0.5V to 2.5V		25		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			20		μV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			50		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		fA/°C
Output Voltage High	V_{OH}	I_L=10mA	2.85	2.92		V
		−40°C≤T_A ≤+85°C	2.8			V
Output Voltage Low	V_{OL}	I_L=10mA		60	100	mV
		−40°C≤T_A ≤+85°C			125	mV
Output Current	I_{OUT}			±250		mA
Closed-Loop Output impedance	Z_{OUT}	f=1MHz, A_V=1		60		Ω
Power Supply Rejection Ratio	PSRR	V_S=3V to 6V	45	55		dB
Supply Current/Amplifier	I_{SY}	V_O=0V		0.7	1	mA
		−40°C≤T_A ≤+85°C			1.25	mA
Slew Rate	SR	R_L=2kΩ		3.5		V/μs
Settling Time	t_S	To 0.01%		1.6		μs
Gain Bandwidth Product	GBP			2.2		MHz
Phase Margin	ΦO			70		Degrees
Channel Separation	CS	f=1kHz, R_L=2kΩ		65		dB

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Voltage Noise Density	e_n	f=1kHz		45		nV/√Hz
		f=10kHz		30		nV/√Hz
Current Noise Density	i_n	f=1kHz		0.05		pA/√Hz

6.2 Electrical characteristics

V_S=5V, V_{CM}=2.5V, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Offset Voltage	V_{OS}				25	mV
		−40°C≤T_A ≤+85°C			30	mV
Input Bias Current	I_B			5	50	pA
		−40°C≤T_A ≤+85°C			60	pA
Input Offset Current	I_{OS}			1	25	pA
		−40°C≤T_A ≤+85°C			30	pA
Input Voltage Range			0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM}=0V to 5V	38	47		dB
Large Signal Voltage Gain	A_{VO}	R_L=2kΩ, V_O=0.5V to 4.5V	15	80		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C≤T_A ≤+85°C		20		μV/°C
Bias Current Drift	$\Delta I_B/\Delta T$			50		fA/°C
Offset Current Drift	$\Delta I_{OS}/\Delta T$			20		fA/°C
Output Voltage High	V_{OH}	I_L=10mA	4.9	4.94		V
		−40°C≤T_A ≤+85°C	4.85			V
Output Voltage Low	V_{OL}	I_L=10mA		50	100	mV
		−40°C≤T_A ≤+85°C			125	mV
Output Current	I_{OUT}			±250		mA
Closed-Loop Output impedance	Z_{OUT}	f=1MHz, A_V=1		40		Ω
Power Supply Rejection Ratio	PSRR	V_S=3V to 6V	45	55		dB
Supply Current/Amplifier	I_{SY}	V_O=0V		0.75	1.25	mA
		−40°C≤T_A ≤+85°C			1.75	mA
Slew Rate	SR	R_L=2kΩ		5		V/μs
Full-Power Bandwidth	BW_p	1% distortion		350		kHz
Settling Time	t_S	To 0.01%		1.4		μs
Gain Bandwidth Product	GBP			3		MHz
Phase Margin	ΦO			70		Degrees

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Channel Separation	CS	f=1kHz, R_L=2kΩ		65		dB
Voltage Noise Density	e_n	f=1kHz		45		nV/√Hz
		f=10kHz		30		nV/√Hz
Current Noise Density	i_n	f=1kHz		0.05		pA/√Hz

7.1 Typical Characteristic

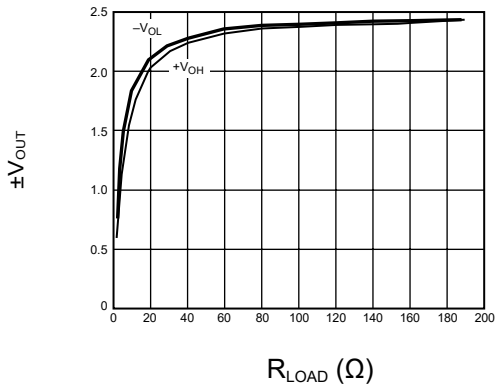


Figure 1: Output Voltage vs. Load, V_S=±2.5 V, R_{LOAD} Is Connected to GND (0V)

7.2 Typical Characteristic

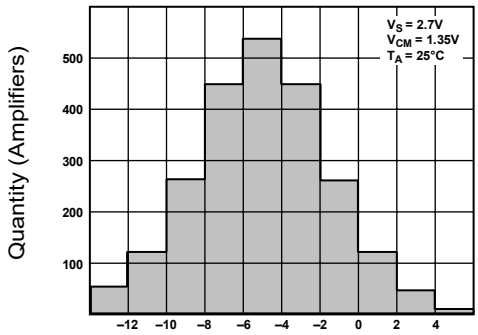


Figure 1: Input Offset Voltage Distribution

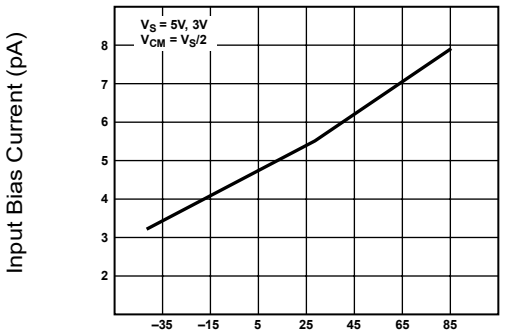


Figure 2: Input Bias Current vs. Temperature

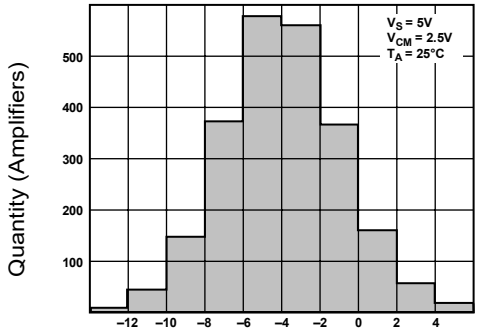


Figure 3: Input Offset Voltage Distribution

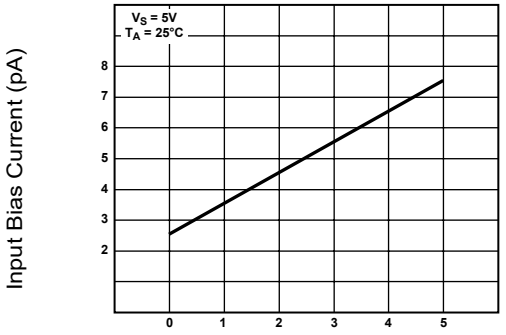


Figure 4: nput Bias Current vs. Common-Mode Voltage

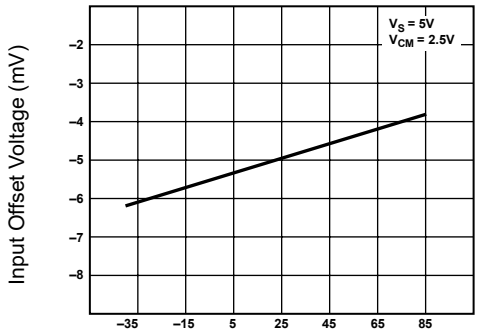


Figure 5: Input Offset Voltage vs. Temperature

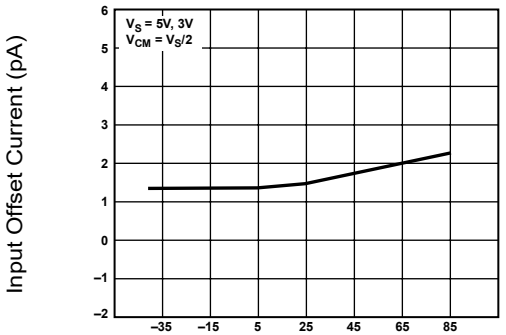


Figure 6: Input Offset Current vs. Temperature

7.3 Typical Characteristic

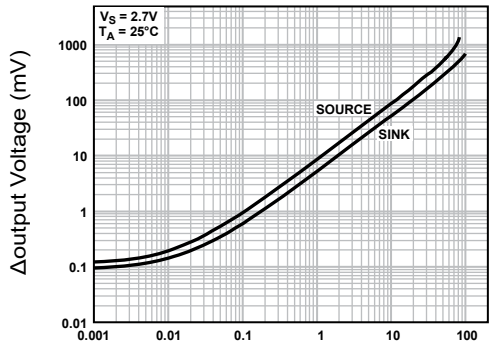


Figure 7: Output Voltage to Supply Rail vs. Load Current

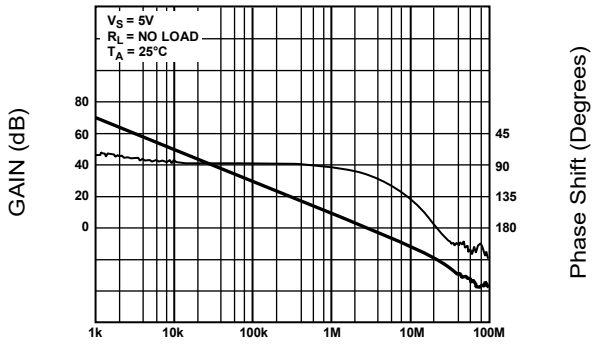


Figure 8: Open-Loop Gain and Phase Shift vs. Frequency

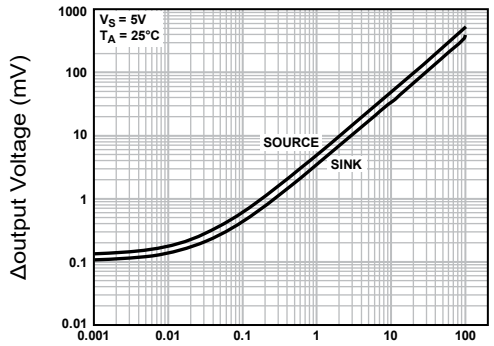


Figure 9: Output Voltage to Supply Rail vs. Load Current

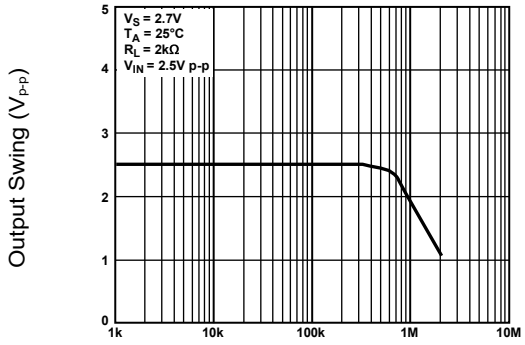


Figure 10: Closed-Loop Output Swing vs. Frequency

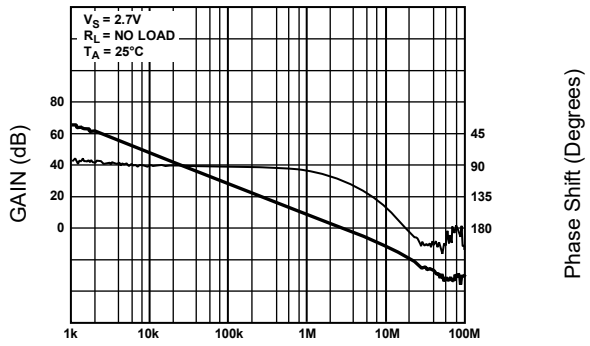


Figure 11: Open-Loop Gain and Phase Shift vs. Frequency

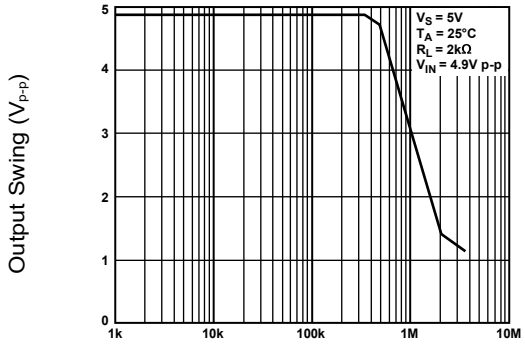


Figure 12: Closed-Loop Output Swing vs. Frequency

7.4 Typical Characteristic

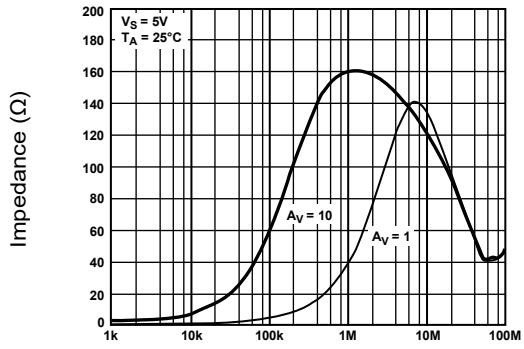


Figure 13: Closed-Loop Output Impedance vs. Frequency

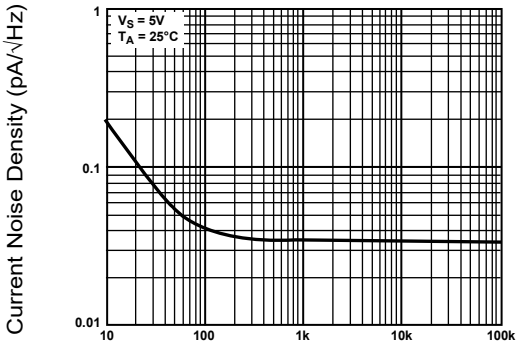


Figure 14: Current Noise Density vs. Frequency

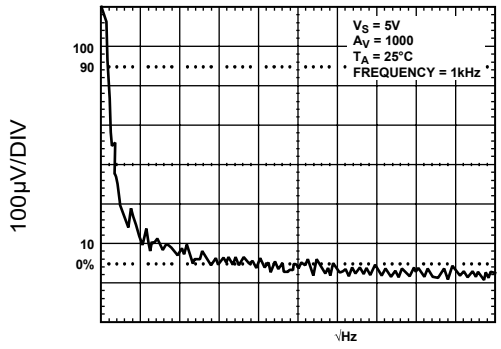


Figure 15: Voltage Noise Density vs. Frequency (1 kHz)

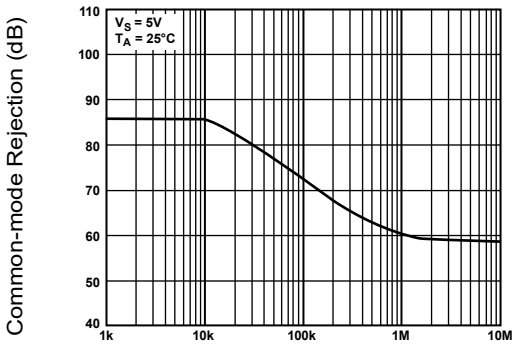


Figure 16: Common-Mode Rejection vs. Frequency

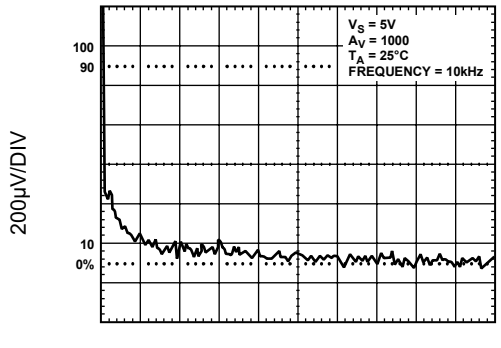


Figure 17: Voltage Noise Density vs. Frequency (10 kHz)

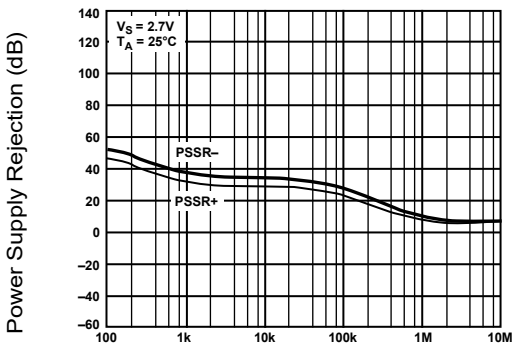


Figure 18: Power Supply Rejection vs. Frequency

7.5 Typical Characteristic

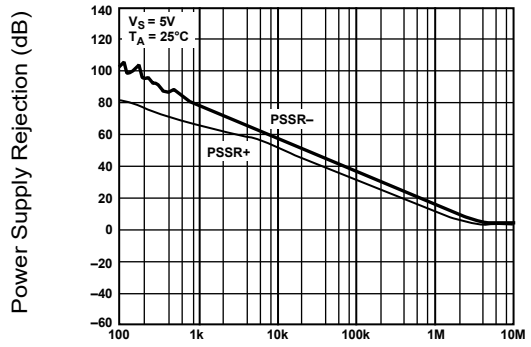


Figure 19: Power Supply Rejection vs. Frequency

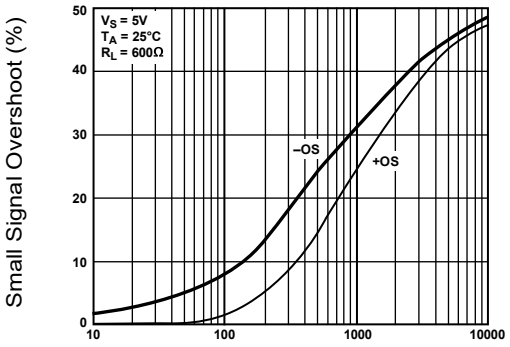


Figure 20: Small Signal Overshoot vs. Load Capacitance

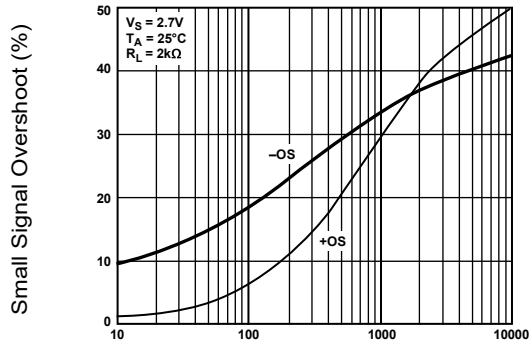


Figure 21: Small Signal Overshoot vs. Load Capacitance

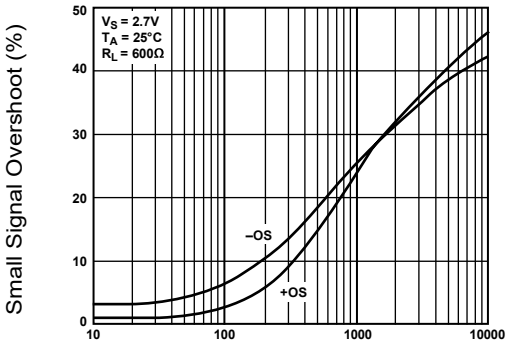


Figure 22: Small Signal Overshoot vs. Load Capacitance

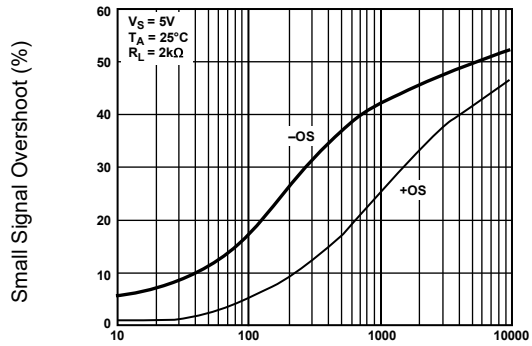


Figure 23: Small Signal Overshoot vs. Load Capacitance

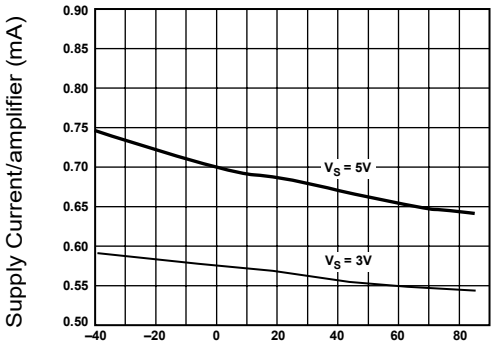


Figure 24: Supply Current per Amplifier vs. Temperature

7.6 Typical Characteristic

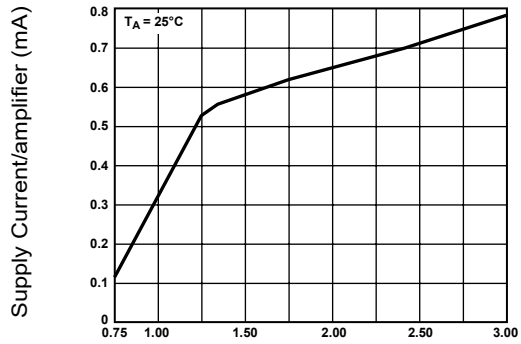


Figure 25: Supply Current per Amplifier vs. Supply Voltage

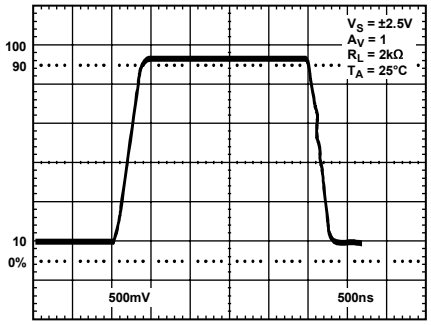


Figure 26: Large Signal Transient Response

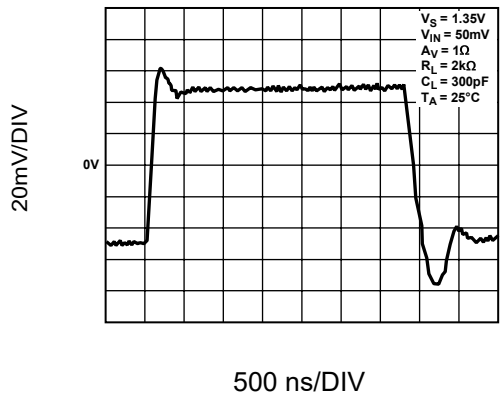


Figure 27: Small Signal Transient Response

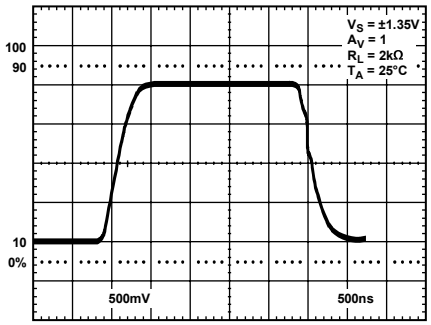


Figure 28: Large Signal Transient Response

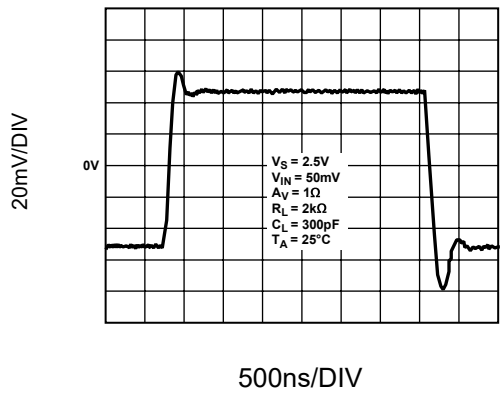


Figure 29: Small Signal Transient Response

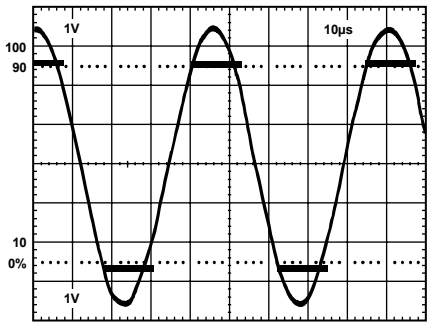
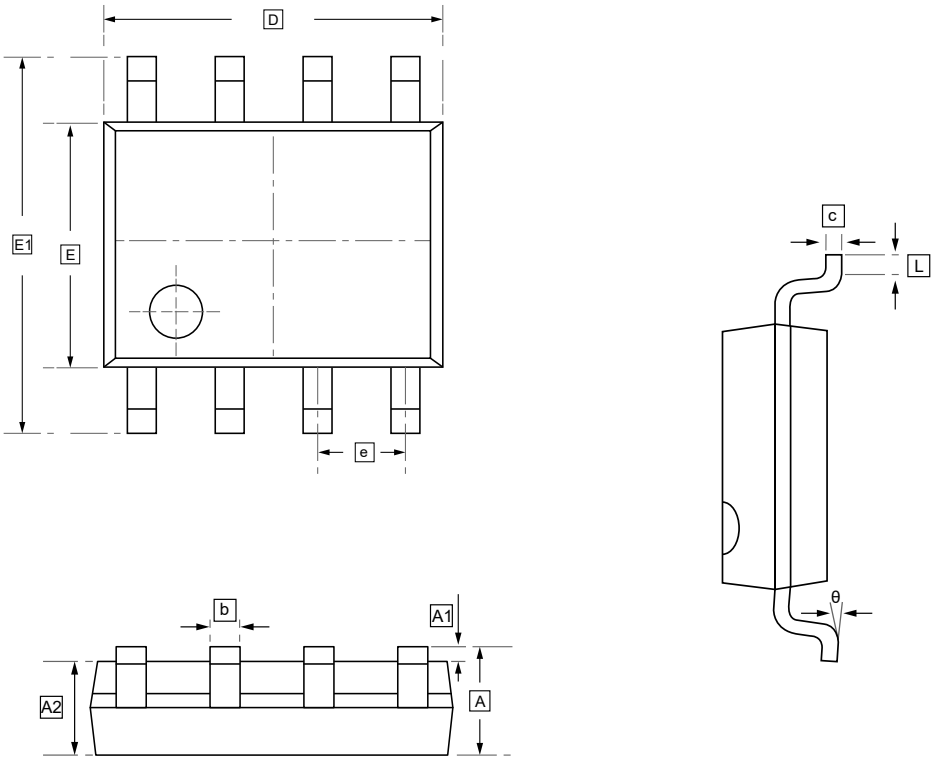


Figure 30: No Phase Reversal

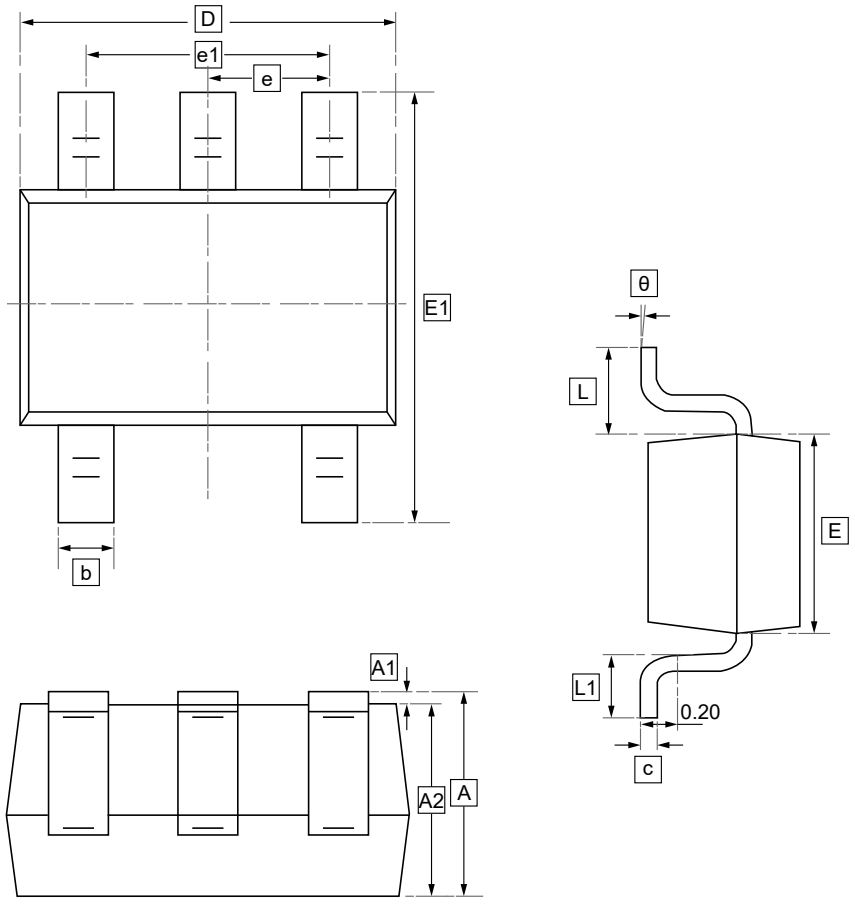
8.1 SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

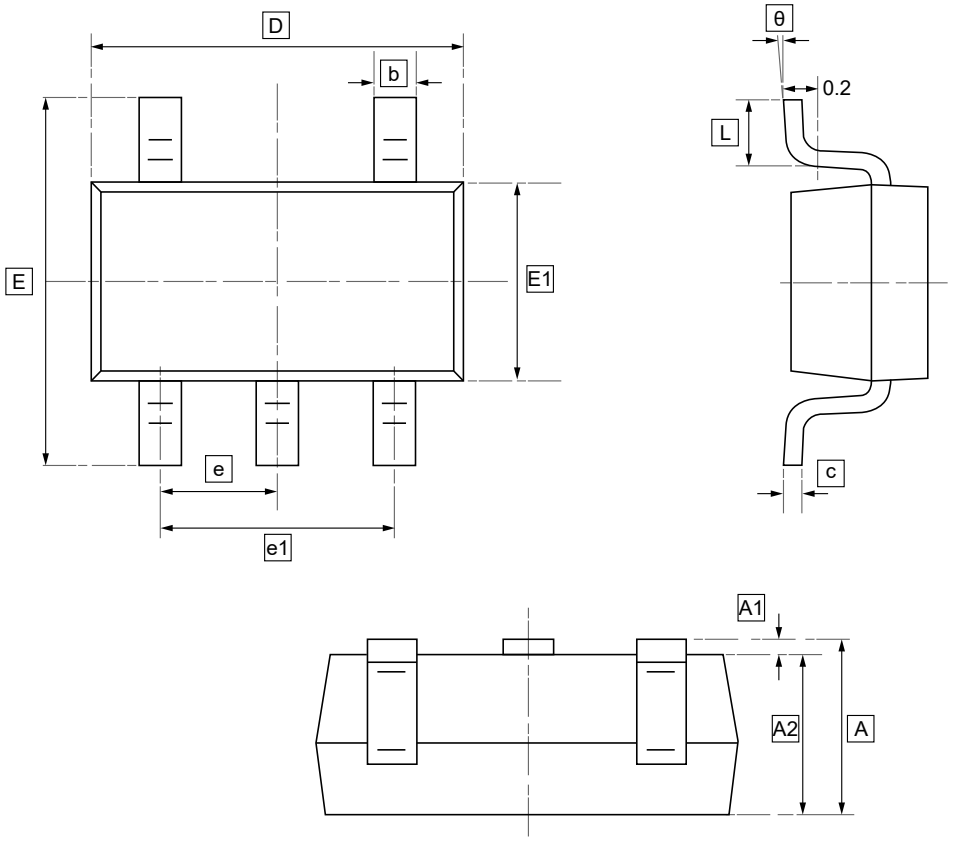
8.2 SC70-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	θ
Min	0.90	0.00	0.90	0.15	0.08	1.80	1.15	2.15	0.65	1.20	0.26	7°
Max	1.10	0.10	1.00	0.35	0.15	2.25	1.35	2.45	TYP	1.40	0.46	REF.

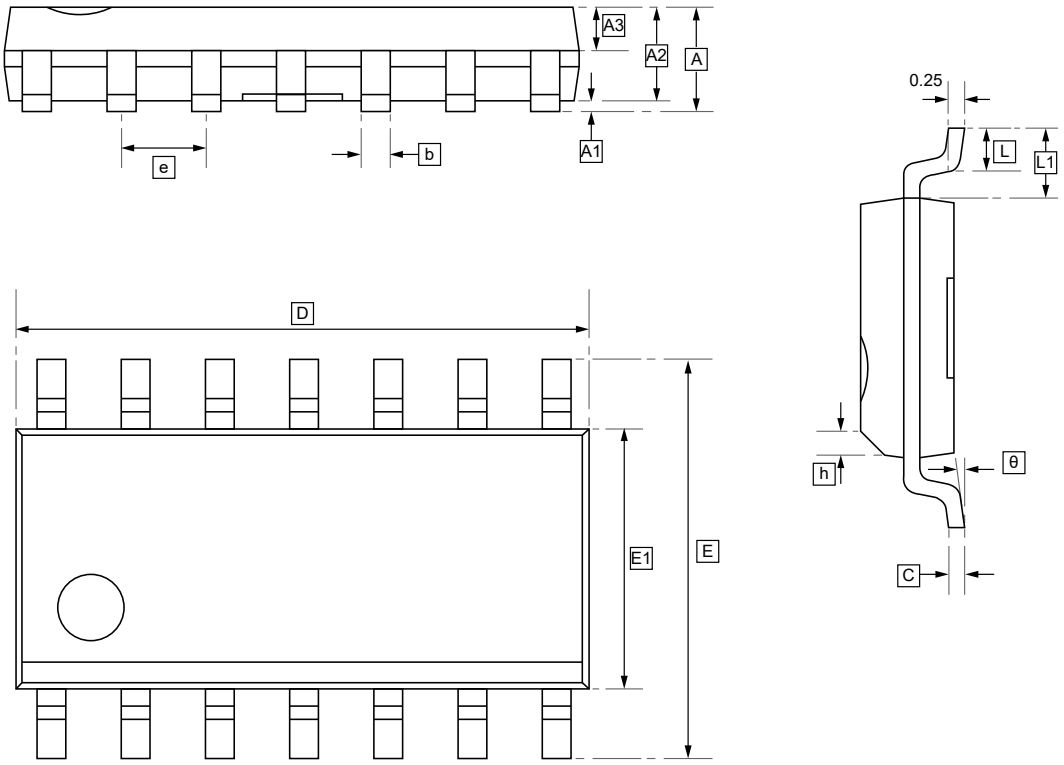
8.3 SOT23-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E1	E	e	e1	L	θ
Min	1.050	0.000	1.050	0.300	0.100	2.820	1.500	2.650	0.950	1.800	0.300	0°
Max	1.250	0.100	1.150	0.500	0.200	3.020	1.700	2.950	BSC	2.000	0.600	8°

8.4 SOP-14 Package Outline Dimensions

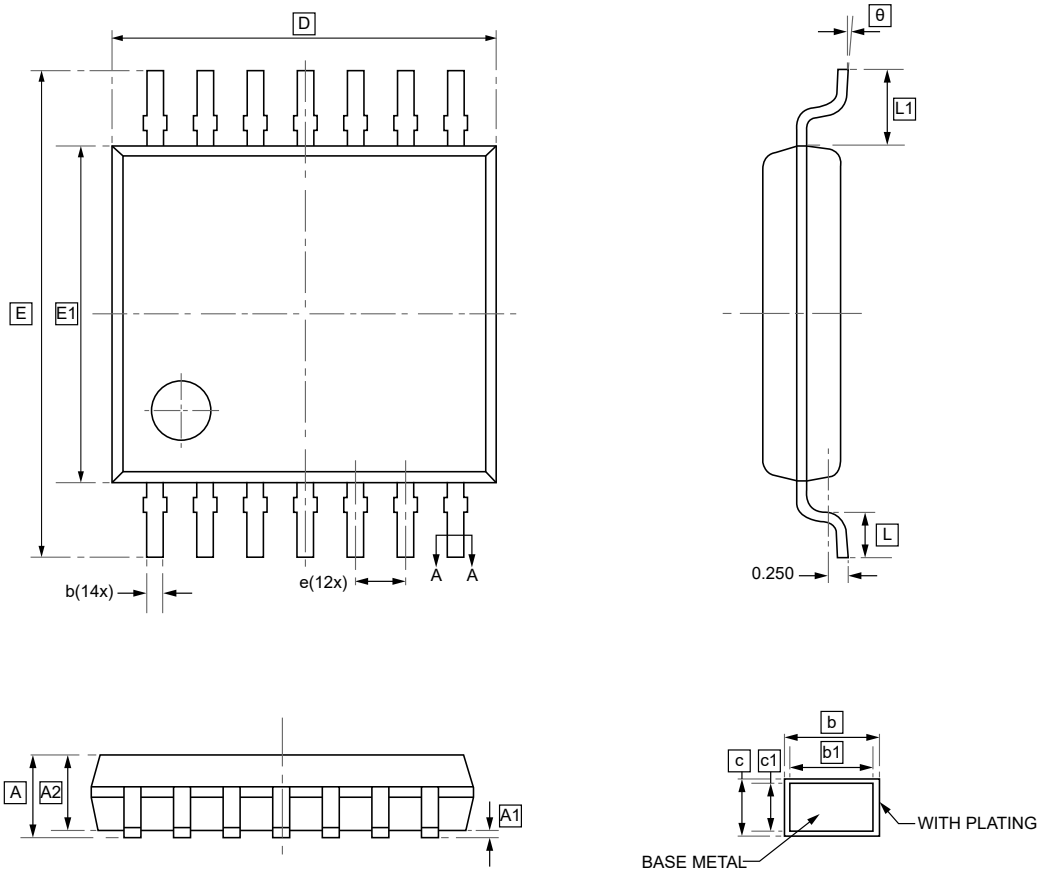


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	C	D	E	E1	e	h	L
Min	-	0.05	1.35	0.65	0.203	0.17	8.45	5.80	3.80	1.24	0.25	0.40
Max	1.75	0.25	1.55	0.75	0.305	0.25	8.85	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

8.5 TSSOP-14 Package Outline Dimensions

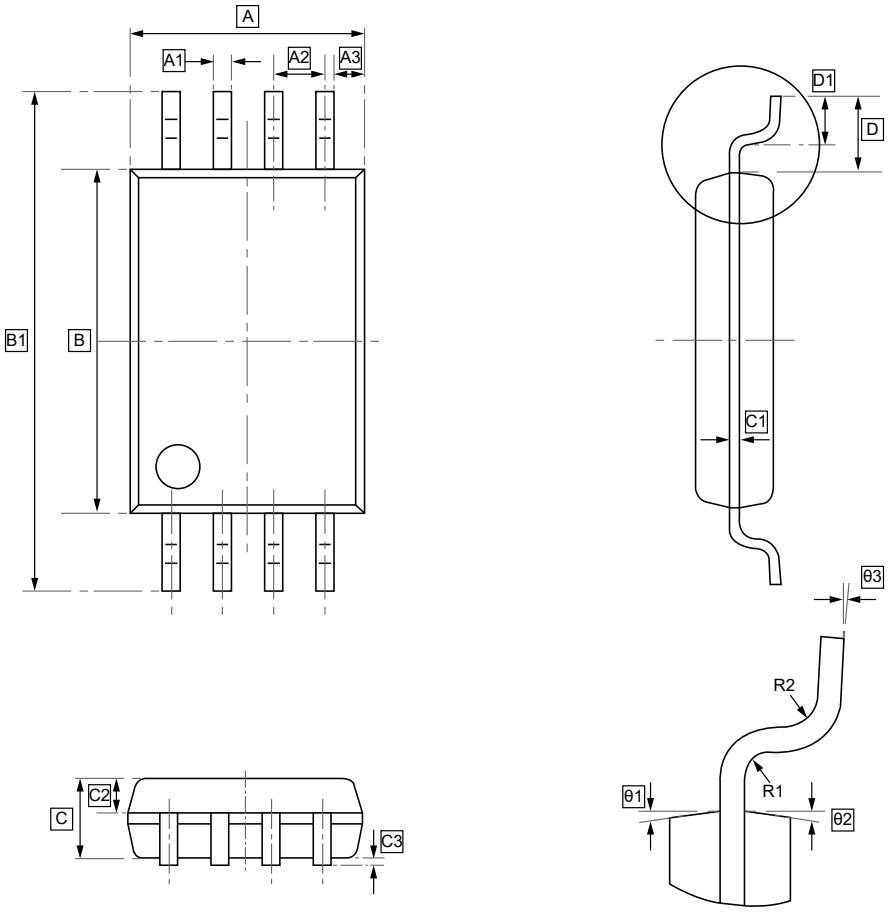


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	b1	c	c1	D	E	E1	e	L1
Min	-	0.05	0.90	0.20	0.19	0.13	0.120	4.90	6.20	4.30	0.65	0.85
Max	1.20	0.15	1.05	0.28	0.25	0.17	0.14	5.10	6.60	4.50	BSC	1.15

Symbol	L	θ
Min	0.45	0°
Max	0.75	8°

8.6 TSSOP-8 Package Outline Dimensions



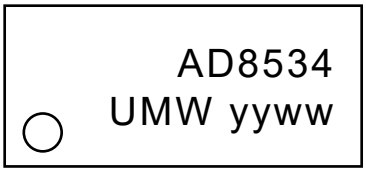
DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	B	B1	C	C1	C2	C3	D	D1
Min	2.90	0.20	0.65	0.36	4.30	6.30	0.95	0.127	0.39	0.05	1.00	0.50
Max	3.10	0.30	TYP	0.46	4.50	6.50	1.05	TYP	0.49	0.15	REF	0.70

Symbol	R1	R2	θ1	θ2	θ3
Min	0.15	0.15	12°	12°	0°
Max	TYP	TYP	TYP4	TYP4	7°

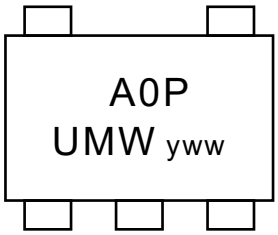
9.Ordering information

SOP-14/TSSOP-14



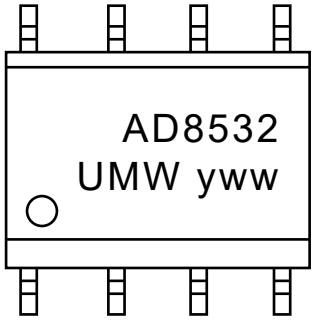
yy: Year Code
ww: Week Code

SOT23-5



y: Year Code
ww: Week Code

SOP-8/TSSOP-8



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW AD8531ARZ	AD8531	SOP-8	2500	Tape and reel
UMW AD8532ARZ	AD8532	SOP-8	2500	Tape and reel
UMW AD8534ARZ	AD8534	SOP-14	2500	Tape and reel
UMW AD8531AKSZ	AOQ	SC70-5	3000	Tape and reel
UMW AD8531ARTZ	A0P	SOT23-5	3000	Tape and reel
UMW AD8532ARUZ	AD8532	TSSOP-8	4000	Tape and reel
UMW AD8534ARUZ	AD8534	TSSOP-14	4000	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.