

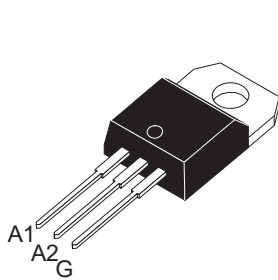
1.Description

NPNN five-layer structure of silicon bidirectional devices; with independent intellectual property rights of single-sided digging technology, table glass passivation process; multi-layer metallized electrodes on the back; with high blocking voltage and high temperature stability

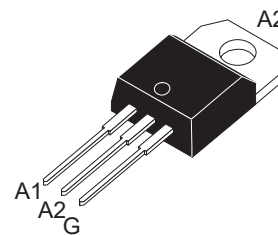
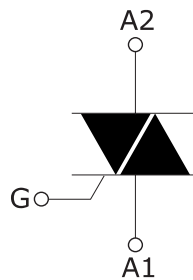
2.Features

vacuum cleaners, power tools and other motor speed controllers; solid state relays; heating controllers (temperature regulation); other phase control circuits.

3.Pinning Information



**TO-220AB
insulated
BTA12**



**TO-220AB
BTB12**



4. Absolute maximum ratings ($T_J=25^{\circ}\text{C}$ unless otherwise stated)

Parameter			Symbol	Values	Units
RMS on-state current (full sine wave)	BTA	T _C =80°C	I _{T(RMS)}	12	A
	BTA	T _C =80°C			
Non repetitive surge peak on-state current (full cycle, T _J initial=25°C)	F=50HZ, tp=20ms		I _{TSM}	120	A
I ² t value for fusing	tp=10ms		I ² t	72	A ² S
Critical rate of rise of on-state current I _G =2 x I _{GT} , tr≤100ns	T _J =125		di/dt	50	A/us
Off state repetitive peak voltage Reverse repetitive peak voltage	T _J =25°C		V _{DRM} /V _{RRM}	600/800	V
Peak gate current	tp=20us	T _J =150°C	I _{GM}	4	A
Average gate power dissipation		T _J =150°C	P _{G(AV)}	1	W
Storage junction temperature range			T _{STG}	-40 to 150	°C
Operating junction temperature range			T _J	-40 to 125	°C



5.1 Electrical characteristics (3 quadrants)

Parameter	Quadrant	Range	Symbol	Values				Units
$V_D=12V$ $R_L=30\Omega$	I	MAX	I_{GT}	BW	CW	SW	TW	mA
		MAX		50	35	10	5	mA
$V_D=V_{DRM}$, $R_L=3.3k\Omega$, $T_J=125^\circ C$	II	MAX	V_{GT}	1.5				V
	III	MIN	V_{GD}	0.2				V
$I_T=100mA$		MAX	I_H	60	40	20	15	mA
$I_G=1.2 \times I_{GT}$		MAX	I_L	100	60	40	30	mA
$V_D = 67\% V_{DRM}$, gate open, mA, $T_J=125^\circ C$		MIN	dv/dt	500	500	200	100	V/us
Critical rise rate of commutation voltage $T_J=150^\circ C$		MIN	(dv/dt)c	8				V/us

5.2 Electrical characteristics (4 quadrants)

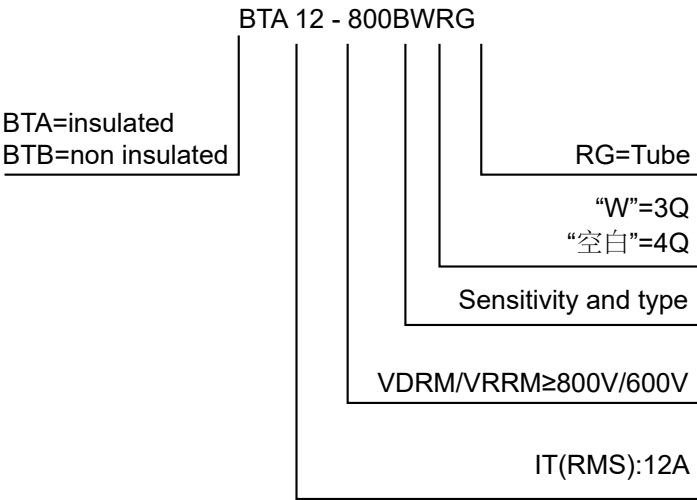
Parameter	Quadrant	Range	Symbol	Values		Units
				B	C	
$V_D=12V$ $R_L=30\Omega$	I - II - III	MAX	I_{GT}	50	20	mA
	IV	MAX		100	60	mA
	ALL	MAX	V_{GT}	1.5		V
$V_D=V_{DRM}$, $R_L=3.3k\Omega$, $T_J=125^\circ C$	ALL	MIN	V_{GD}	0.2		V
$I_T=500mA$		MAX	I_H	60	50	mA
$I_G=1.2 \times I_{GT}$	I - IV - III	MAX	I_L	60	50	mA
	II	MAX		100	80	mA
$V_D = 67\% V_{DRM}$, gate open, mA, $T_J=125^\circ C$		MIN	dv/dt	500		V/us
Critical rise rate of commutation voltage $T_J=150^\circ C$		MIN	(dv/dt)c	10		V/us



6.Static Parameters

Parameter			Symbol	Values	Units
$I_{TM}=24A$	$T_J=25^{\circ}C$	MAX	V_{TM}	1.5	V
threshold on-state voltage	$T_J=150^{\circ}C$	MAX	V_{T0}	0.86	V
Dynamic resistance	$T_J=150^{\circ}C$	MAX	R_d	36.6	mΩ
$V_{DRM}=V_{RRM}$	$T_J=25^{\circ}C$	MAX	I_{DRM}, I_{RRM}	5	uA
	$T_J=125^{\circ}C$	MAX		1	mA
Junction to ambient	BTA	MAX	$R_{th(j-c)}$	2.05	°C/W
	BTB	MAX		1.25	°C/W

7.Static Parameters





8.1 Typical Characteristic

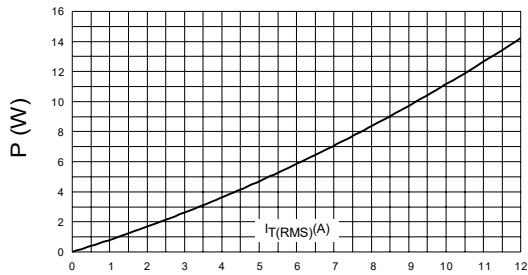


Figure 1: Maximum power dissipation versus on-state RMS current (full cycle)

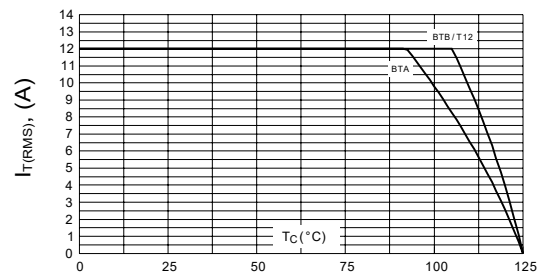


Figure 2: RMS on-state current versus case temperature (full cycle)

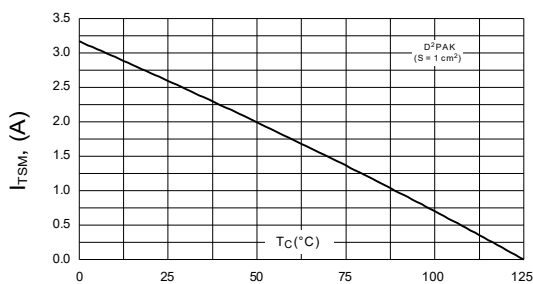


Figure 3: RMS on-state current versus ambient temperature (printed circuit board FR4, copper thickness: 35 μm) (full cycle)

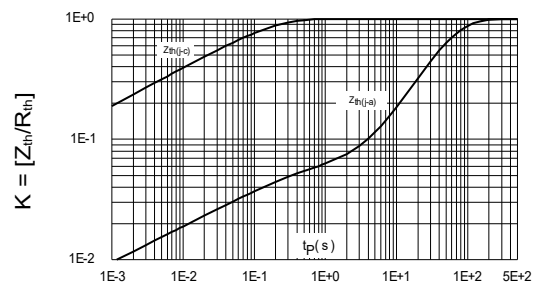


Figure 4: Relative variation of thermal impedance versus pulse duration

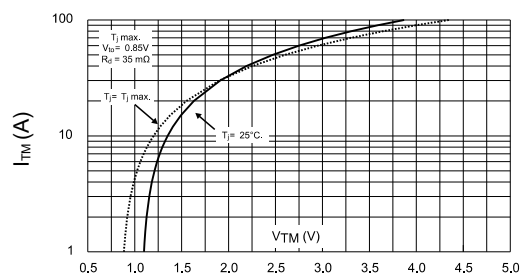


Figure 5: On-state characteristics (maximum values)

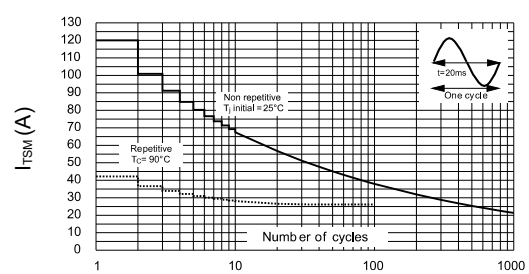


Figure 6: Surge peak on-state current versus number of cycles



8.2 Typical Characteristic

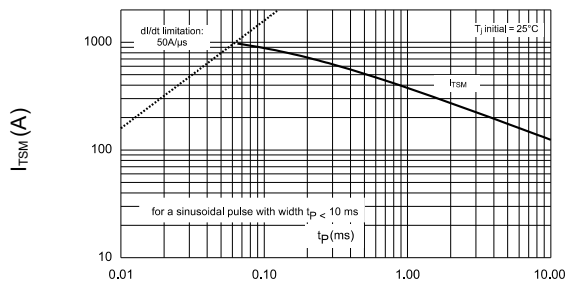


Figure 7: Non-repetitive surge peak on-state current

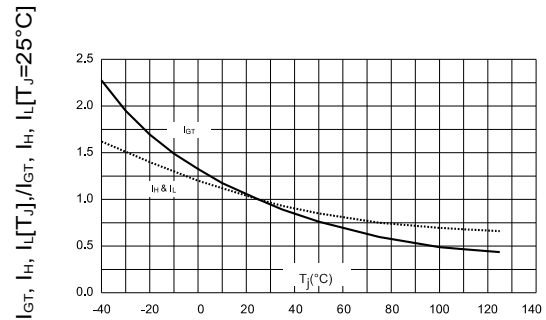


Figure 8: Relative variation of gate trigger current, holding current and latching current versus junction temperature (typical values)

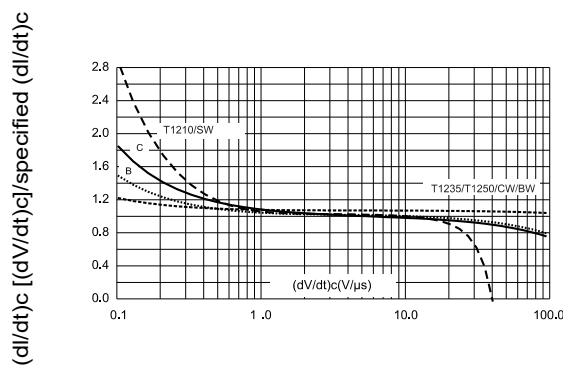


Figure 9: Relative variation of critical rate of decrease of main current versus $(dV/dt)_C$ (typical values)

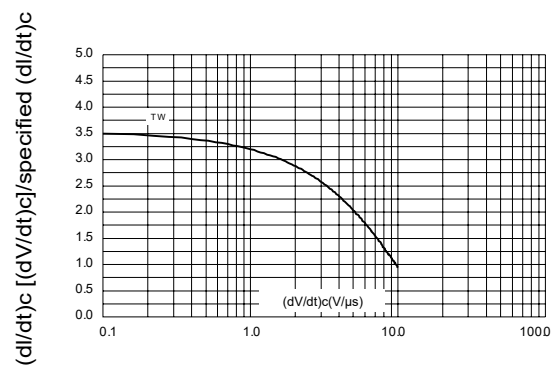


Figure 10: Relative variation of critical rate of decrease of main current versus $(dV/dt)_C$ (typical values) (TW)

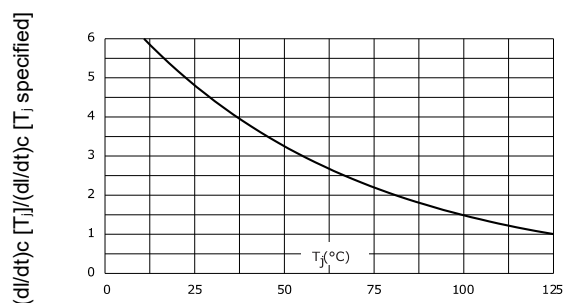


Figure 11: Relative variation of critical rate of decrease of main current versus junction temperature

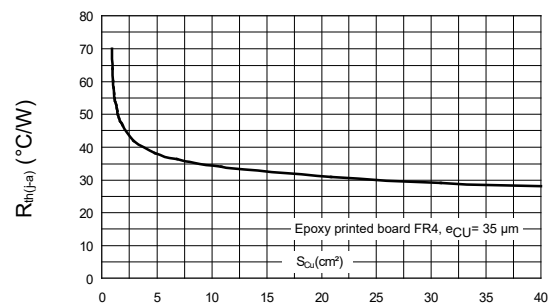
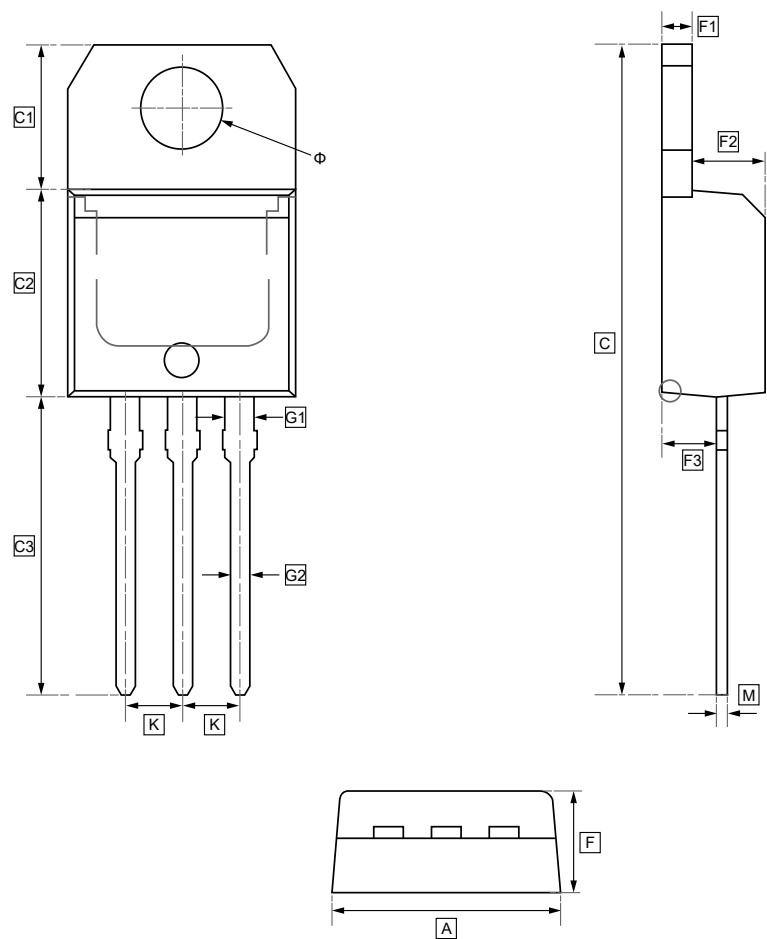


Figure 12: Thermal resistance junction to ambient versus copper surface under tab (printed circuit board FR4, copper thickness: 35μm)



9.1 TO-220A Package Outline Dimensions



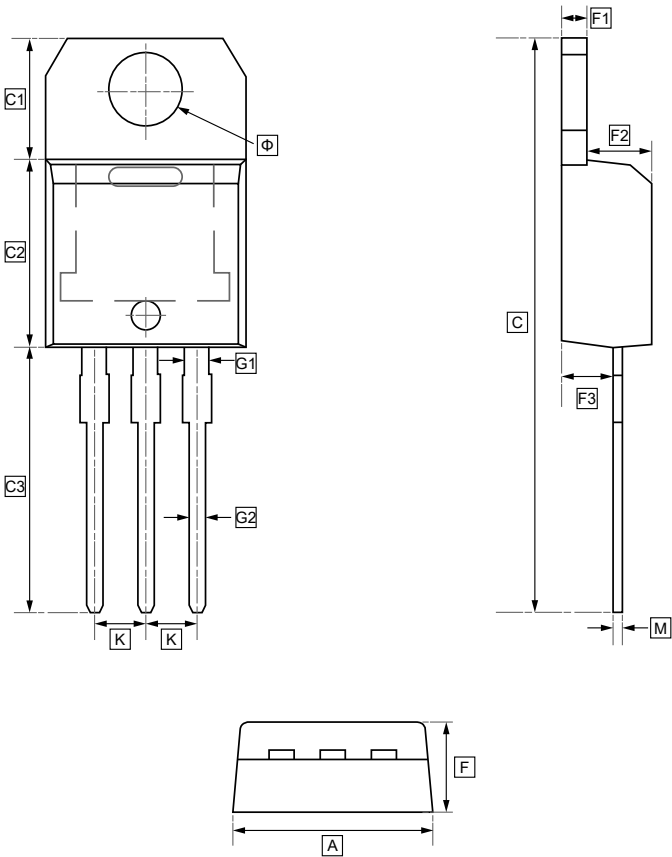
DIMENSIONS (mm are the original dimensions)

Symbol	A	C	C1	C2	C3	Φ	F	F1	F2	F3	G1	G2
Min	10.000	28.700	6.400	9.040	13.160	3.700	4.350	1.220	3.130	2.300	1.220	0.750
Max	10.200	29.100	6.500	9.240	13.460	3.800	4.650	1.320	3.330	2.700	1.320	0.850

Symbol	M	K
Min	0.450	2.540
Max	0.550	



9.2 TO-220B Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	C	C1	C2	C3	Φ	F	F1	F2	F3	G1	G2
Min	9.900	28.600	6.100	9.240	13.160	3.700	4.320	1.200	3.120	2.300	1.200	0.750
Max	10.100	29.000	6.200	9.440	13.460	3.800	4.620	1.300	3.320	2.700	1.300	0.850

Symbol	M	K
Min	0.400	2.540
Max	0.500	



10. Ordering Information

BTA12-600B
UMW yyww

yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW BTA12-600BRG	BTA12-600B	TO-220A	1000	Tube and box
UMW BTA12-600CRG	BTA12-600C	TO-220A	1000	Tube and box
UMW BTA12-800BRG	BTA12-800B	TO-220A	1000	Tube and box
UMW BTA12-800CRG	BTA12-800C	TO-220A	1000	Tube and box
UMW BTA12-600BWRG	BTA12-600BW	TO-220A	1000	Tube and box
UMW BTA12-600CWRG	BTA12-600CW	TO-220A	1000	Tube and box
UMW BTA12-800BWRG	BTA12-800BW	TO-220A	1000	Tube and box
UMW BTA12-800CWRG	BTA12-800CW	TO-220A	1000	Tube and box
UMW BTA12-600SWRG	BTA12-600SW	TO-220A	1000	Tube and box
UMW BTA12-600TWRG	BTA12-600TW	TO-220A	1000	Tube and box
UMW BTA12-800SWRG	BTA12-800SW	TO-220A	1000	Tube and box
UMW BTB12-600BRG	BTB12-600B	TO-220B	1000	Tube and box
UMW BTB12-600CWRG	BTB12-600CW	TO-220B	1000	Tube and box
UMW BTB12-600BWRG	BTB12-600BW	TO-220B	1000	Tube and box
UMW BTB12-800CWRG	BTB12-800CW	TO-220B	1000	Tube and box
UMW BTB12-800BWRG	BTB12-800BW	TO-220B	1000	Tube and box



11.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

When reselling, applying, or exporting, please comply with export control laws and regulations of China, the United States, the United Kingdom, the European Union, and other relevant countries, regions, and international organizations.

This document and any actions by UMW do not grant any intellectual property rights, whether express or implied, by estoppel or otherwise. The product names and marks mentioned herein may be trademarks of their respective owners.