UMW TLV521DCKR

NanoPower, 350nA, RRIO, CMOS Input, Operational Amplifier

1.Description

The UMW TLV521DCKR 350 nA nanopower op amp offers optimum price performance in TI's nanopower family of operational amplifiers. The UMW TLV521DCKR has a carefully designed CMOS input stage enabling very low Ibias of 1pA thereby reducing IBIAS and IOS errors that would otherwise impact sensitive applications like Mega-ohm resistance, high-impedance photodiode and charge sense situations. Additionally, built-in EMI protection reduces sensitivity to unwanted RF signals from sources like mobile phones and RFID readers. The UMW TLV521 is offered in the 5-pin SC70 package,and operates from –40°C to 125°C.

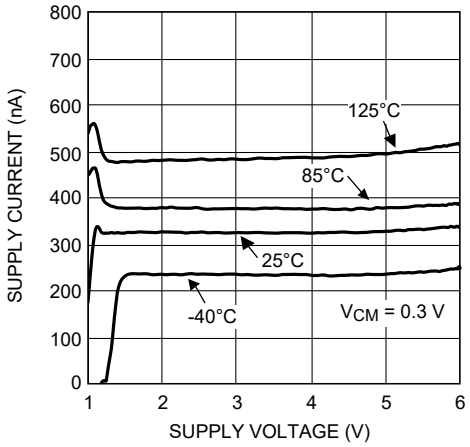
2.Applications

- Wireless Remote Sensors
- Powerline Monitoring
- Power Meters
- Battery Powered Industrial Sensors
- Micropower Oxygen Sensor and Toxic Gas Sensor
- Active RFID Readers
- Zigbee Based Sensors for HVAC Control
- Sensor Network Powered by Energy Scavenging
- Current Sensing
- Glucose Monitoring

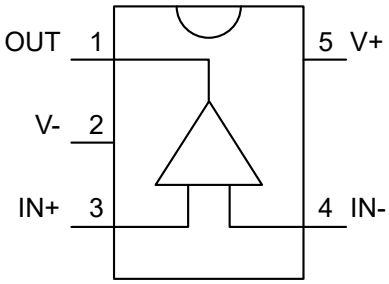
3.Features

- Unmatched Price Performance
- For V_S=3.3V, Typical Unless Otherwise Noted
- – Ultra-low Supply Current
- – 350nA Typical, 500 nA Maximum
- – Wide Operating Voltage Range 1.7V to 5.5V
- – Low TCV_{OS} 1.5μV/°C
- – V_{OS} 3 mV(Max)
- – Input Bias Current 1pA
- – PSRR 100dB
- – CMRR 90dB
- – Open-Loop Gain 110dB
- – Gain Bandwidth Product 6 kHz
- – Slew Rate 2.5V/ms
- – Input Voltage Noise at f=100Hz 300nV/√Hz
- – Temperature Range –40ºC to 125°C
- – Rail to Rail Input and Output (RRIO)

4.Nanopower Supply Current



5.Pinning information



SC70-5

Pin Functions:

Pin		I/O	Description
NO.	Name		
1	OUT	O	Output
2	V-	P	Negative Power Supply
3	IN+	I	Noninverting Input
4	IN-	I	Inverting input
5	V+	P	Positive Power Supply

6.Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Symbol	Min	Max	Units
Any pin relative to V-			-0.3	6	V
IN+, IN-, OUT Pins			V^--0.3V	V^++0.3V	V
V^+, V^-, OUT Pins				40	mA
Differential input Voltage		V_{IN+}-V_{IN-}	-300	300	mV
Junction Temperature			-40	150	°C
Mounting Temperature	Infrared or Convection (30 sec.)			260	°C
	Wave Soldering Lead Temp.(4 sec.)			260	°C
Storage temperature		T_{STG}	-65	150	°C

Notes:

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.ESD Ratings

Parameter		Symbol	Value	Units
Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	$V_{(ESD)}$	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	
	Machine Model		±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter	Min	Max	Units
Temperature Range	-40	125	°C
Supply Voltage (V_S=V^+-V^-)	1.7	5.5	V

(1) Absolute Maximum Ratings indicate limits beyond which damage may occur. Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but specific performance is not ensured. For ensured specifications and test conditions, see Electrical Characteristics.

9.Thermal Information (TLV521)

Thermal Metric(1)	Symbol	DCK (SC70)	Units
		5 Pins	
Junction-to-ambient thermal resistance	$R_{\theta JA}$	269.9	°C/W
Junction-to-case (top) thermal resistance	$R_{\theta JC(top)}$	93.7	°C/W
Junction-to-board thermal resistance	$R_{\theta JB}$	48.8	°C/W
Junction-to-top characterization parameter	Ψ_{JT}	2	°C/W
Junction-to-board characterization parameter	Ψ_{JB}	47.9	°C/W
Junction-to-case (bottom) thermal resistance	$R_{\theta JC(bot)}$	N/A	°C/W

10.1 Electrical Characteristics

Unless otherwise specified, all limits for T_A=25°C, V^+=3.3 V, V^-=0 V, V_{CM}=V_O=V^+/2, and R_L>1MΩ.(1)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Offset Voltage	V_{OS}	V_{CM}=0.3V	-3	0.1	3	mV
		V_{CM}=3V	-3	0.1	3	mV
Input Offset Voltage Drift	V_{OS}TC			±1.5		μV/°C
Input Bias Current	I_{BIAS}			1		pA
Input Offset Current	I_{OS}			50		fA
Common Mode Rejection Ratio	CMRR	0V≤V_{CM}≤3.3V	70	90		dB
		0V≤V_{CM}≤2.2V		10		dB
Power Supply Rejection Ratio	PSRR	V^+=1.8V to 3.3V, V_{CM}=0.3V	80	100		dB
Common Mode Voltage Range	CMVR	CMRR≥70dB	0		3.3	V
Large Signal Voltage Gain	A_{VOL}	V_O=0.5V to 2.8V, R_L=100kΩ to V^+/2	80	110		dB
Output Swing High	V_O	R_L=100kΩ to V^+/2, $V_{IN(diff)}$=100mV		3	50	mV from either rail
Output Swing Low		R_L=100kΩ to V^+/2, $V_{IN(diff)}$=-100mV		2	50	
Output Current	I_O	Sourcing, V_O to V-, $V_{IN(diff)}$=100mV		11		mA
		Sinking, V_O to V+, $V_{IN(diff)}$=100mV		12		mA
Supply Current	I_S	V_{CM}=0.3V		350	500	nA

10.2 AC Electrical Characteristics (1)

Unless otherwise specified, all limits for T_A=25°C, V^+=3.3 V, V^-=0 V, V_{CM}=V_O=V^+/2, and R_L>1MΩ.(1)

Parameter	Symbol	Conditions		Min(2)	Typ(3)	Max(2)	Units
Gain-Bandwidth Product	GBW	C_L=20pF,, R_L=100kΩ			6		kHz
Slew Rate	SR	AV=+1	Falling Edge		2.9		V/ms
		V_{IN}=0V to 3.3V	Rising Edge		2.5		V/ms
Phase Margin	θ_m	C_L=20pF,, R_L=100kΩ			73		deg
Gain Margin	G_m	C_L=20pF,, R_L=100kΩ			19		dB
Input-Referred Voltage Noise Density	e_n	f=100Hz			300		nV/√Hz
Input-Referred Voltage Noise		0.1Hz to 10Hz			22		μV_{PP}
Input-Referred Current Noise	I_n	f=100Hz			100		fA/√Hz
EMI Rejection Ratio, IN+ and IN- (4)	EMIRR	V_{RF_PEAK}=100mV_P (-20 dBP) f=400MHz			121		dB
		V_{RF_PEAK}=100mV_P (-20 dBP) f=900MHz			121		dB
		V_{RF_PEAK}=100mV_P (-20 dBP) f=1800MHz			124		dB
		V_{RF_PEAK}=100mV_P (-20 dBP) f=2400MHz			142		dB

(1) Electrical Characteristics values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that T_J =T_A. Parametric performance, as indicated in the electrical tables, is not ensured under conditions of self heating where T_J>T_A. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.

(2) All limits are ensured by testing, statistical analysis or design.

(3) Typical values represent the most likely parametric norm at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not ensured on shipped production material.

(4) The EMI Rejection Ratio is defined as EMIRR=20log (V_{RF}_P_{EAK}/ΔV_{OS})

11.1 Typical Characteristic

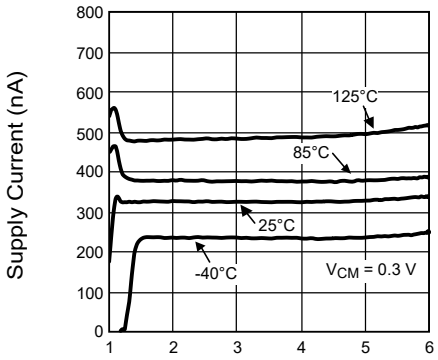


Figure 1: Supply Current vs. Supply Voltage

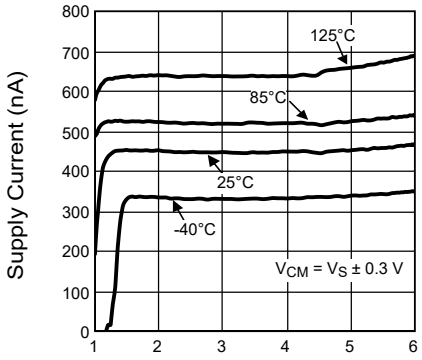


Figure 2: Supply Current vs. Supply Voltag

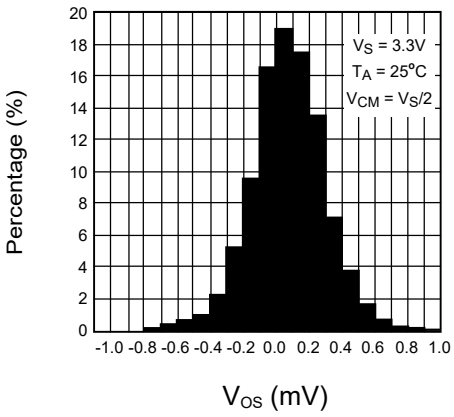


Figure 3: Offset Voltage Distributio

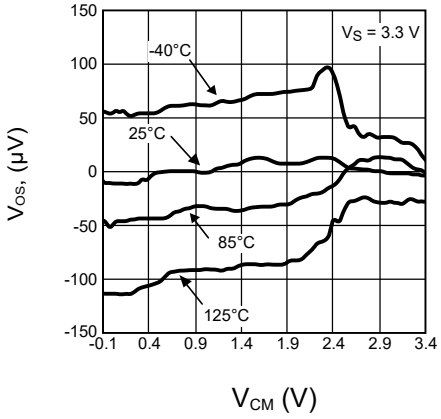


Figure 4: Input Offset Voltage vs. Input Common Mode

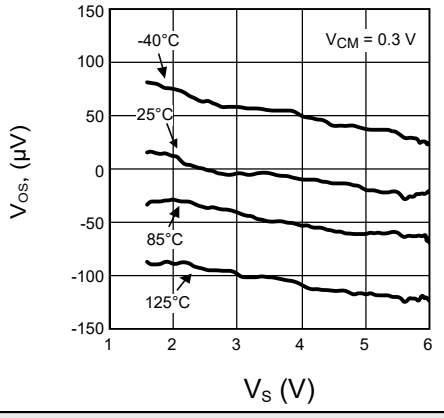


Figure 5: Input Offset Voltage vs. Supply Voltage

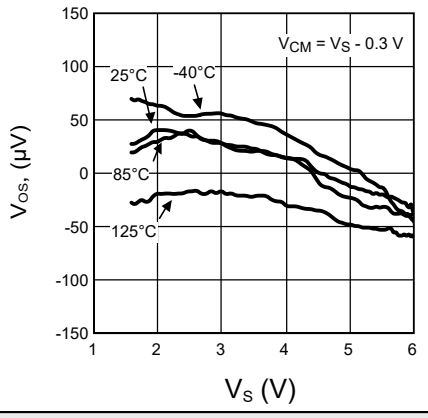


Figure 6: Input Offset Voltage vs. Supply Voltage

11.2 Typical Characteristic

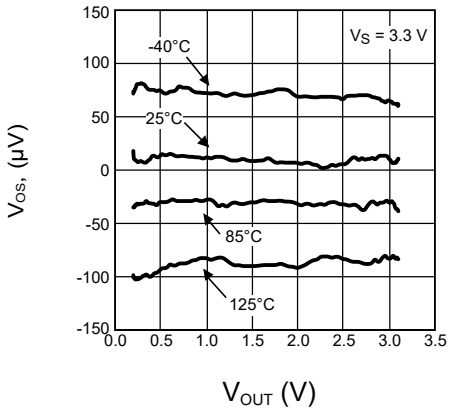


Figure 7: Input Offset Voltage vs. Output Voltage

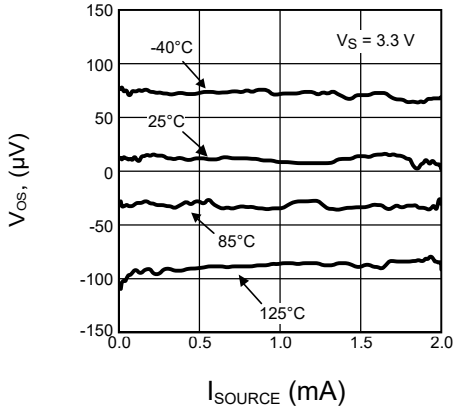


Figure 8: Input Offset Voltage vs. Sourcing Current

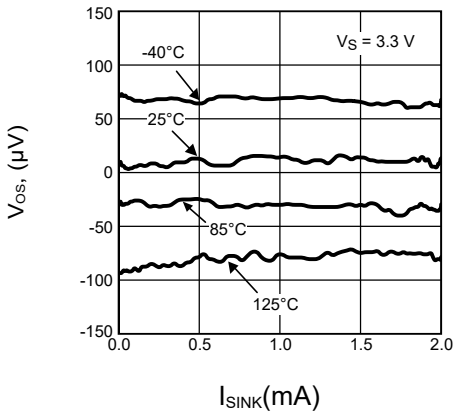


Figure 9: Input Offset Voltage vs. Sinking Current

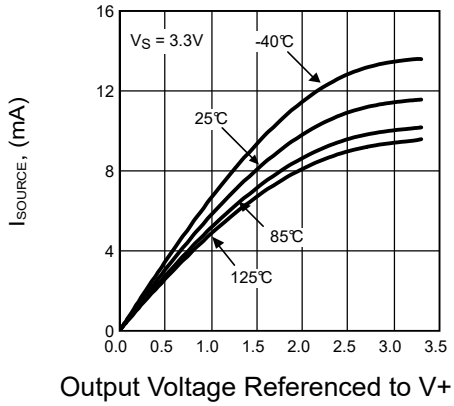


Figure 10: Sourcing Current vs. Output Voltage

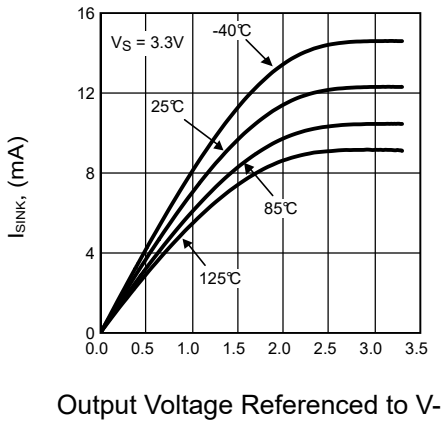


Figure 11: Sinking Current vs. Output Voltage

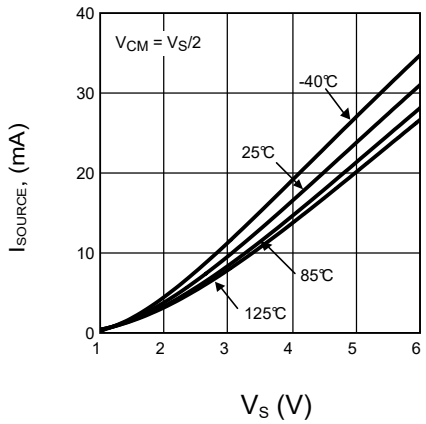


Figure 12: Sourcing Current vs. Supply Voltage

11.3 Typical Characteristic

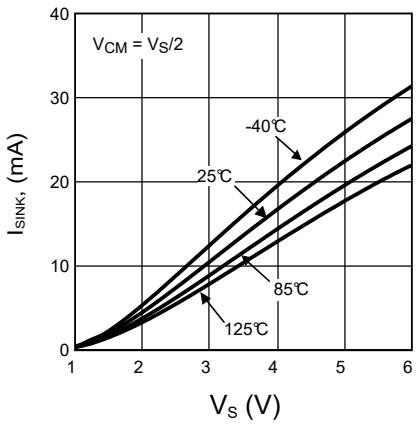


Figure 13: Sinking Current vs. Supply Voltage

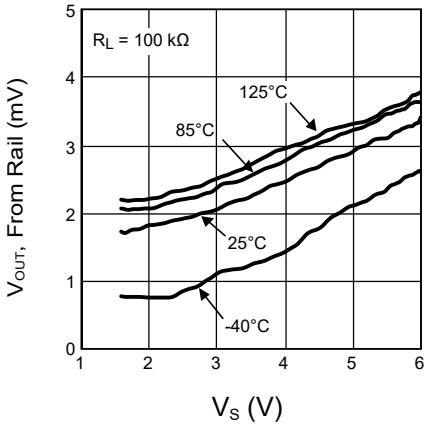


Figure 14: Output Swing High vs. Supply Voltage

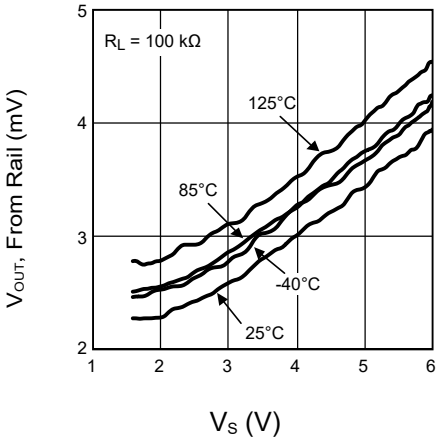


Figure 15: Output Swing Low vs. Supply Voltage

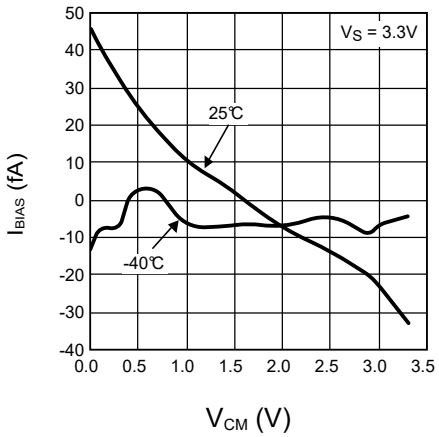


Figure 16: nput Bias Current vs. Common Mode Voltage

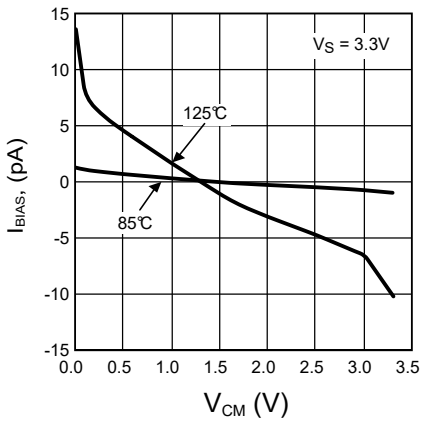


Figure 17: Input Bias Current vs. Common Mode Voltage

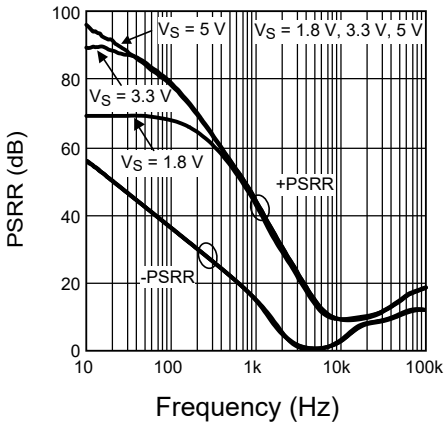


Figure 18: PSRR vs. Frequency

11.4 Typical Characteristic

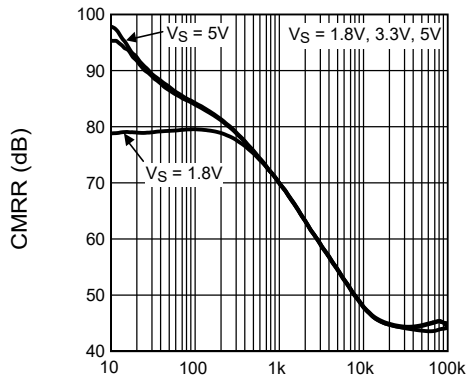


Figure 19: CMRR vs. Frequency

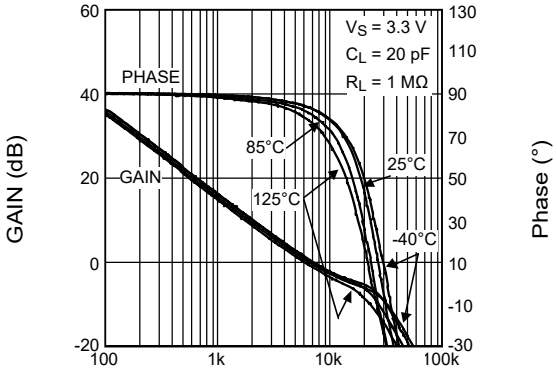


Figure 20: Frequency Response vs. Temperature

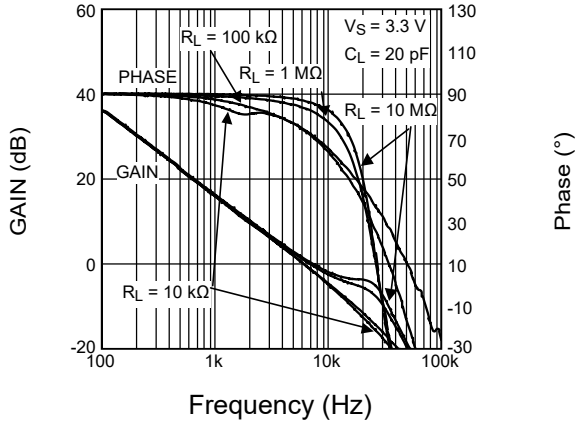


Figure 21: Frequency Response vs. R_L

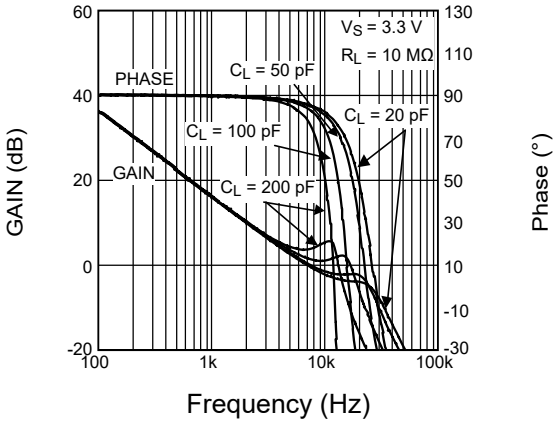


Figure 22: Frequency Response vs. C_L

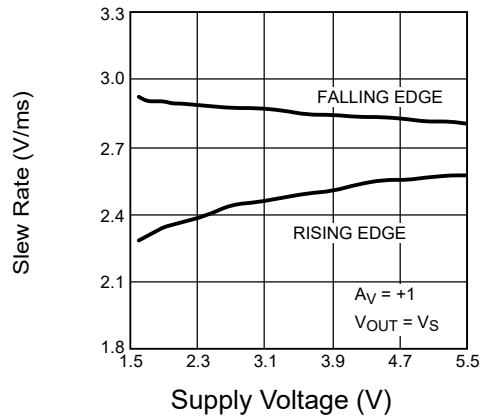


Figure 23: Slew Rate vs. Supply Voltage

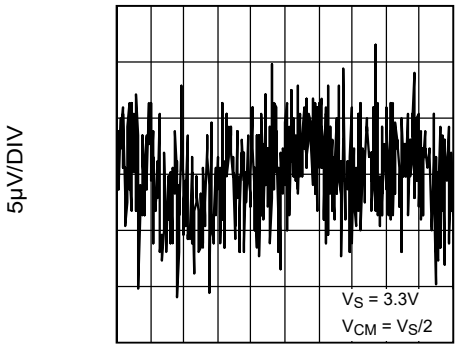


Figure 24: 0.1 to 10 Hz Time Domain Voltage Noise

11.5 Typical Characteristic

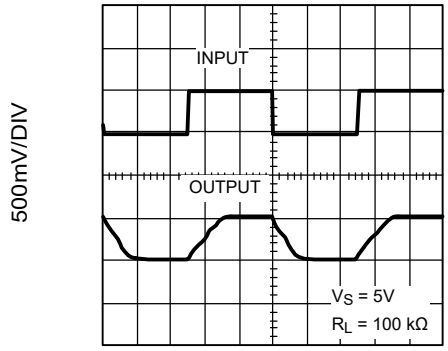


Figure 25: Large Signal Pulse Response

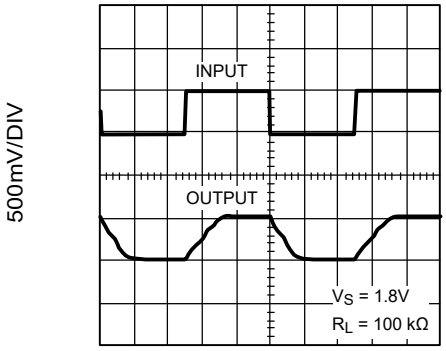


Figure 26: Large Signal Pulse Response

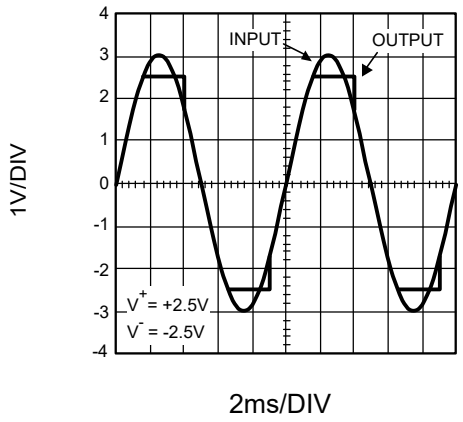


Figure 27: Overload Recovery Waveform

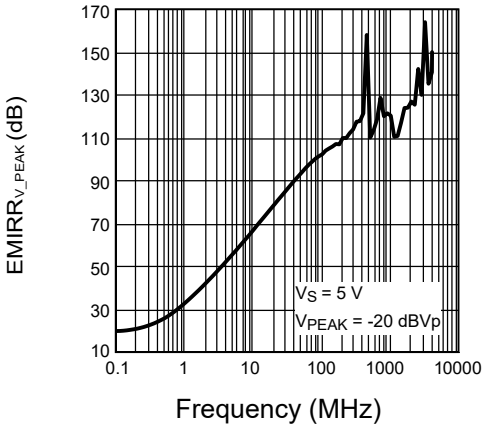
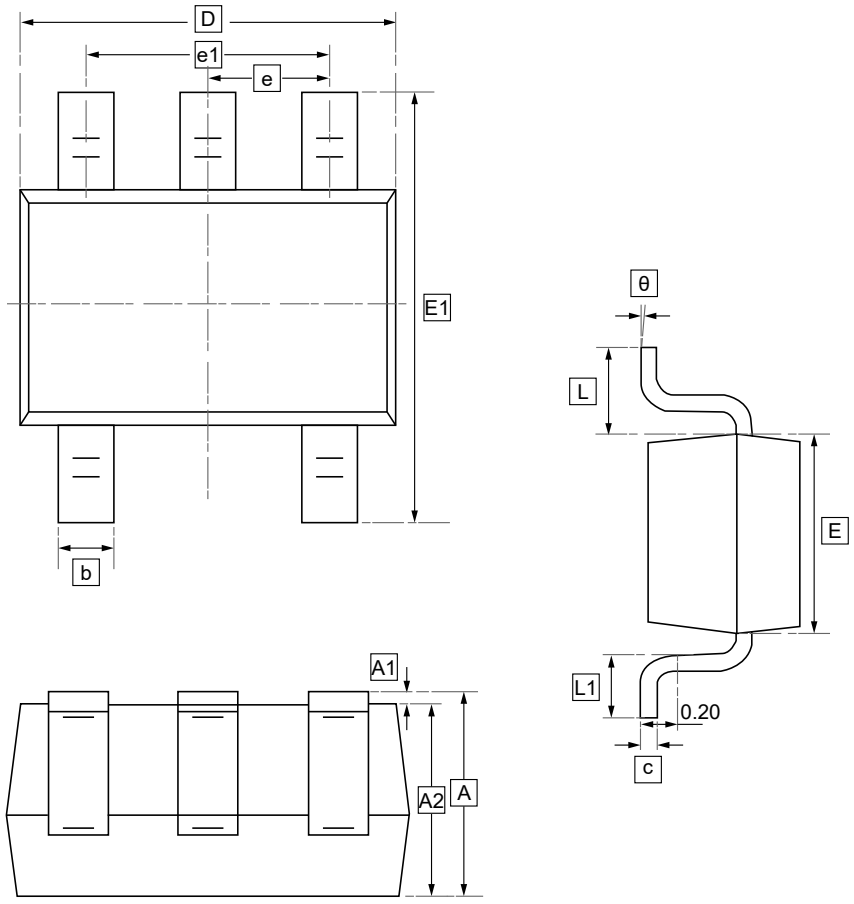


Figure 28: EMIRR vs. Frequency

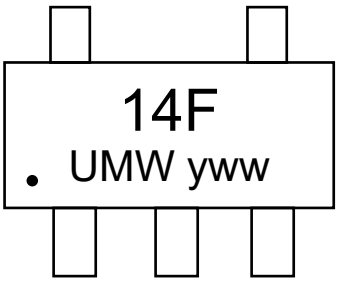
12.SC70-5 (SOT353) Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	θ
Min	0.90	0.00	0.90	0.15	0.08	1.80	1.15	2.15	0.65	1.20	0.26	7°
Max	1.10	0.10	1.00	0.35	0.15	2.25	1.35	2.45	TYP	1.40	0.46	REF.

13.Ordering information



yww: Batch Code

Order Code	Package	Base QTY	Delivery Mode
UMW TLV521DCKR	SC70-5	3000	Tape and reel

14.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

Unless explicitly stated in writing, UMW products are not intended for use in medical, life-saving, or life-sustaining applications, nor for any other applications where product failure could result in personal injury or death. If customers use or sell the product for such applications without explicit authorization, they assume all associated risks.

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