UMW IRLML2803TR

30V N-Channel MOSFET

1.Description

The IRLML2803TR uses advanced trench technology to provide excellent $R_{DS(on)}$ with low gate charge. This device is suitable for use as a loads witch or in PWM applications.

2.Features

- $V_{DS\ (V)}$=30V
- $R_{DS(ON)}$<150mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<200mΩ(V_{GS}=4.5V)

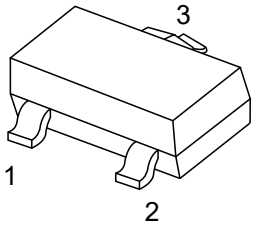
3.Application

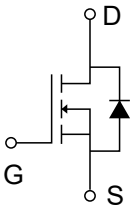
- Generation VTechnology UltraLowOn- Resistance
- Low Profile (<1.1mm)
- Available in Tape and Reel
- Fast Switching
- Lead-Free
- RoHS CompliantHalogen-Free

4.Pinning information

Pin	Symbol	Description
1	G	GATE
2	S	SOURCE
3	D	DRAIN

SOT-23





5.Maximum ratings (T_A=25°C unless otherwise noted)

Parameter		Symbol	Value	Units
Continuous Drain Current, V_{GS} @ 10V	T_A=25°C	I_D	1.2	A
Continuous Drain Current, V_{GS} @ 10V	T_A=70°C		0.93	
Pulsed Drain Current ①		I_{DM}	7.3	
Power Dissipation	T_A=25°C	P_D	540	mW
Linear Derating Factor			4.3	mW/°C
Gate-to-Source Voltage		V_{GS}	±20	V
Single Pulse Avalanche Energy ⑤		E_{AS}	3.9	mJ
Peak diode Recovery dv/dt ②		dv/dt	5	V/ns
Junction and Storage Temperature Range		T_J,T_{STG}	-55 to 150	°C

6.Thermal Resistance Rating

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambien ④	$R_{\theta JA}$		230	°C/W

7.Electrical Characteristics T_J=25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=250μA, V_{GS}=0V	30			V
Breakdown Voltage Temp. Coefficient	$\Delta V_{(BR)DSS}/\Delta T_J$	I_D=1mA, Reference to 25°C		0.029		V/°C
Static Drain-to-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=0.91A ③			150	mΩ
		V_{GS}=4.5V, I_D=0.46A ③			200	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1			V
Forward Transconductance	g_{fs}	V_{DS}=10V, I_D=0.46A	0.87			S
Drain-to-Source Leakage Current	I_{DSS}	V_{DS}=24V,V_{GS}=0V			1	μA
		V_{DS}=24V,V_{GS}=0V,T_J=125°C			25	
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS}=-20V			-100	nA
Gate-to-Source Reverse Leakage		V_{GS}=20V			100	
Total Gate Charge	Q_g	I_D=0.91A		3.3	5	nC
Gate-to-Source Charge	Q_{gs}	V_{DS}=24V		0.48	0.72	
Gate-to-Drain ("Miller") Charge	Q_{gd}	V_{GS}=10V, See Fig.6 and 9 ③		1.1	1.7	
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=15V		3.9		ns
Rise Time	t_r	I_D=0.91A		4		
Turn-Off Delay Time	$t_{D(off)}$	R_G=6.2Ω		9		
Fall Time	t_f	R_D=16Ω, See Fig.10 ③		1.7		
Input Capacitance	C_{iss}	V_{GS}=0V		85		pF
Output Capacitance	C_{oss}	V_{DS}=25V		34		
Reverse Transfer Capacitance	C_{rss}	f=1MHz, See Fig.5		15		

Source-Drain Ratings and Characteristics						
Continuous Source Current (Body Diode)	I_S	MOSFET symbol showing the integral reverse p-n junction diode.			0.54	A
Pulsed Source Current (Body Diode) ①	I_{SM}				7.3	
Diode Forward Voltage	V_{SD}	T_J=25°C,I_S=0.91A,V_{GS}=0V ③			1.2	V
Reverse Recovery Time	t_{rr}	T_J=25°C, I_F=0.91A		26	40	ns
Reverse Recovery Charge	Q_{rr}	dI/dt=100A/μs ③		22	32	nC

Notes:

① Repetitive rating; pulse width limited bymax.junction temperature.(See fig.11)

② I_{SD}≤ 0.91A, di/dt ≤ 120A/μS, V_{DD} ≤ $V_{(BR)DSS}$,T_J≤ 150°C

③ Pulse width ≤ 300us; duty cycle ≤ 2%.

④ Surface mounted on FR-4 board, t≤ 5sec.

⑤ Limited by T_{Jmax}, starting T_J= 25°C,L= 9.4mH, R_G = 25Ω, I_{AS}= 0.9A.

8.1Typical Characterisitics

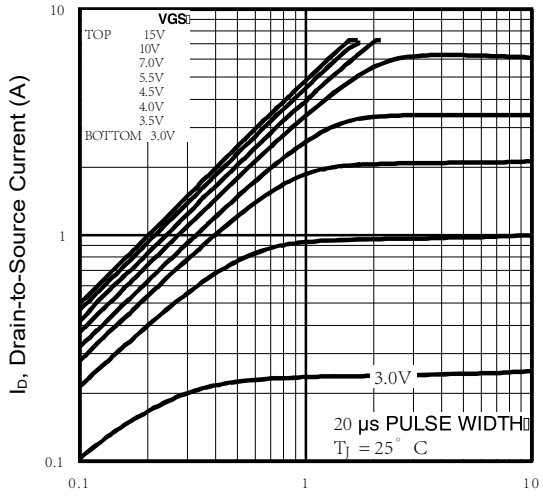


Fig 1. Typical Output Characteristics

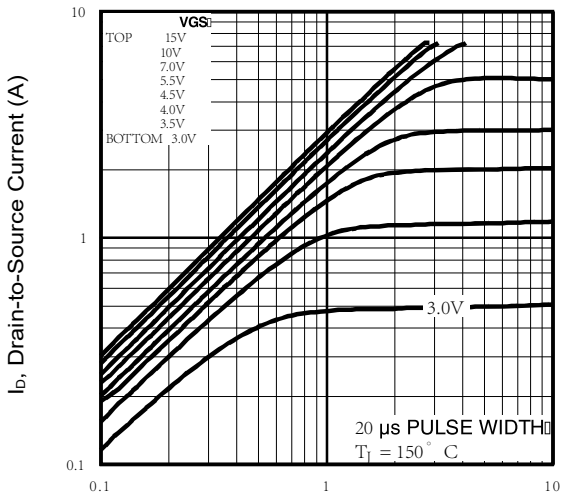


Fig 2. Typical Output Characteristics

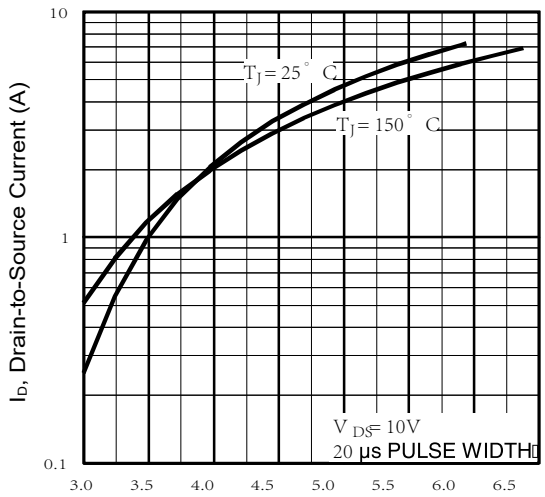


Fig 3. Typical Transfer Characteristics

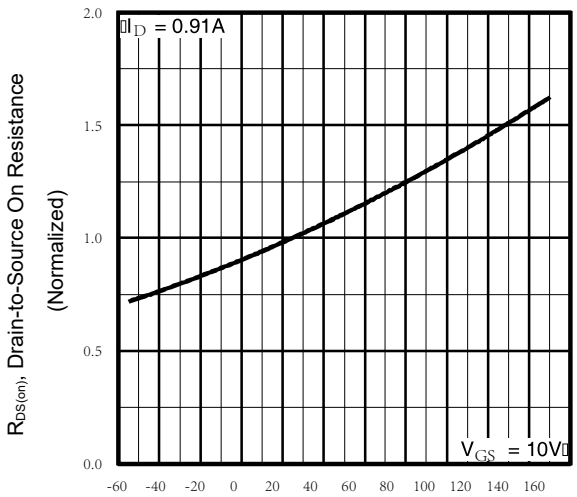
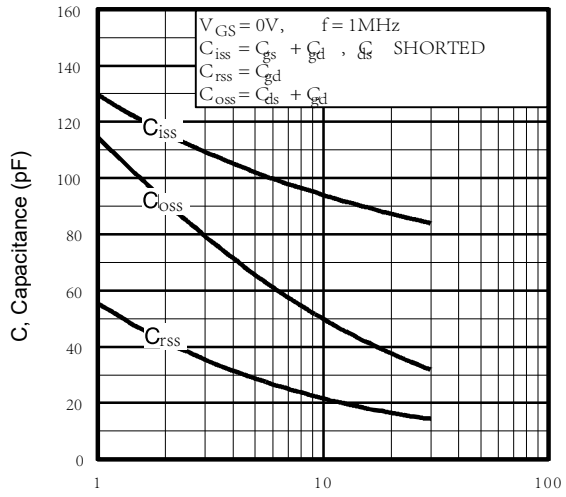


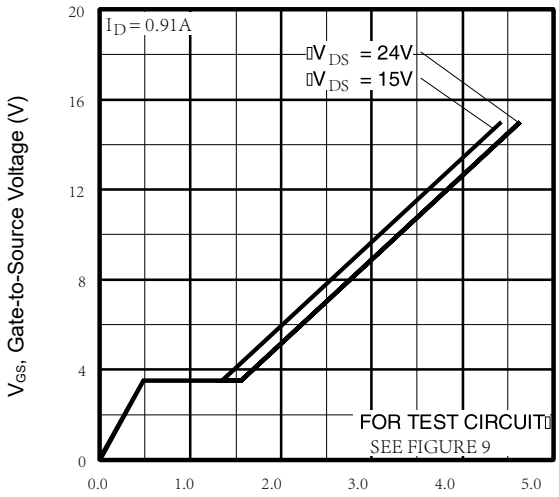
Fig 4. Nomalized On-ResistanceVs. Temperature

8.2Typical Characterisitics



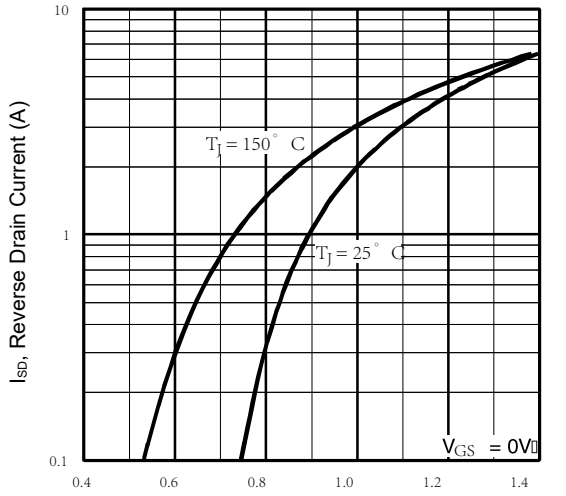
V_{DS} ,Drain-to-Source Voltage (V)

Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage



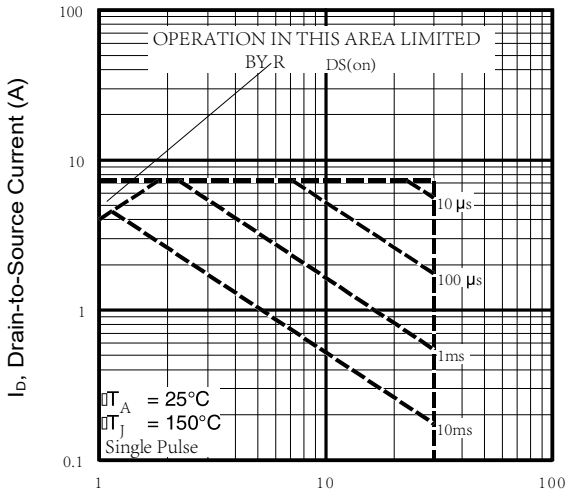
Q_G, Total Gate Charge (nC)

Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage



V_{SD}, Source-to-Drain Voltage (V)

Fig 7. Typical Source-Drain Diode Forward Voltage



V_{DS}, Drain-to-Source Voltage (V)

Fig 8. Maximum Safe Operating Area

8.3Typical Characterisitics

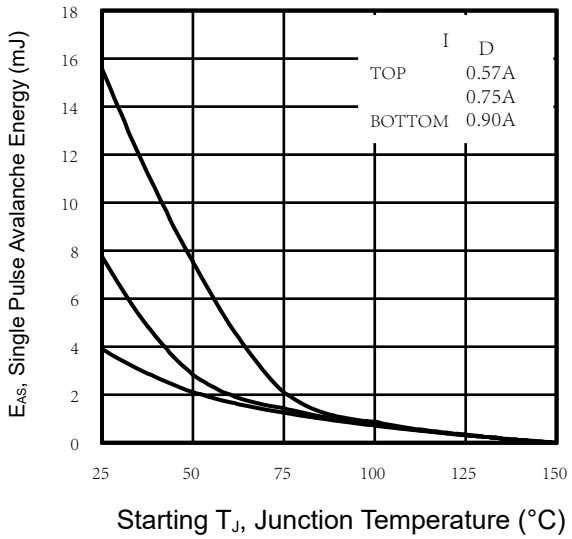


Fig 9. Maximum Avalanche Energy vs. Drain Current

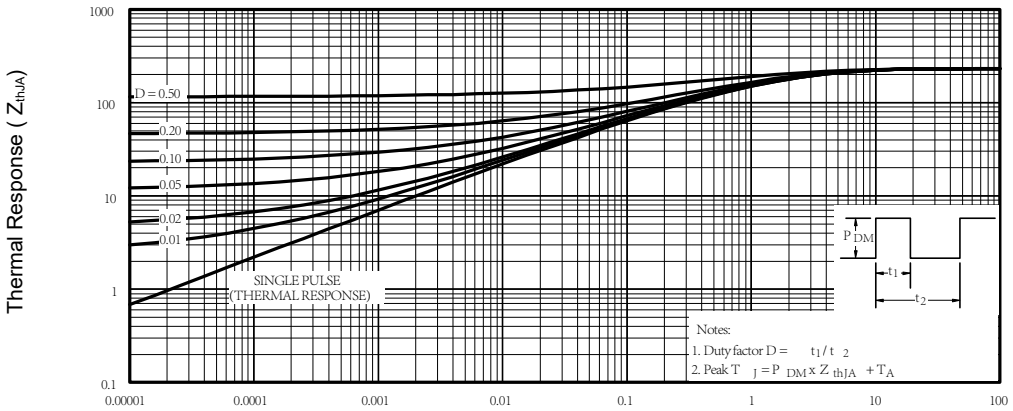


Fig 10. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

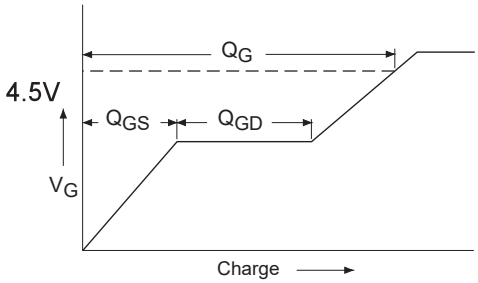


Fig 11a. Basic Gate Charge Wavefomm

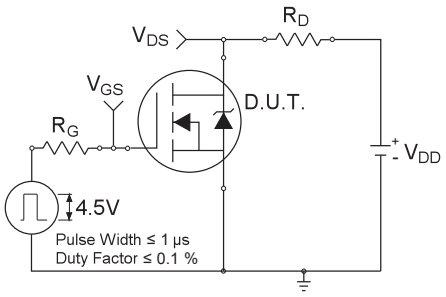


Fig 11a. Switching Time Test Circui

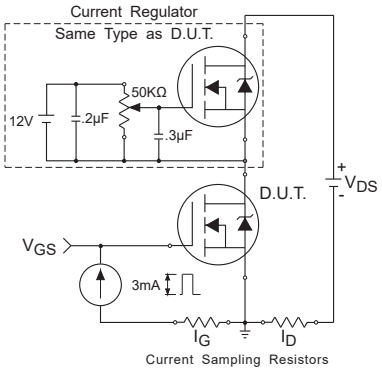


Fig 12a. Gate Charge Test Circuit

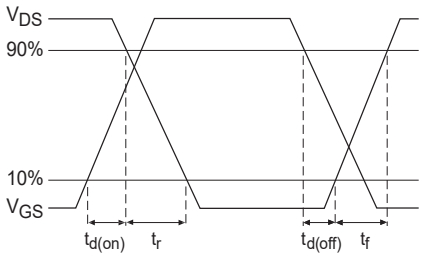


Fig 12b. Switching Time Wavefomms

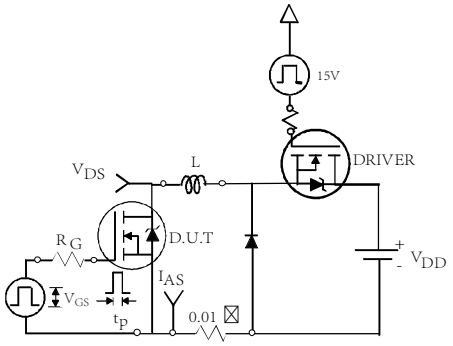


Fig 13a. Unclamped Inductive Test Circuit

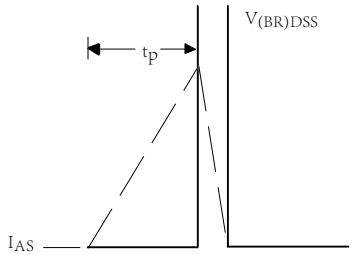


Fig 13b. Unclamped Inductive Waveforms

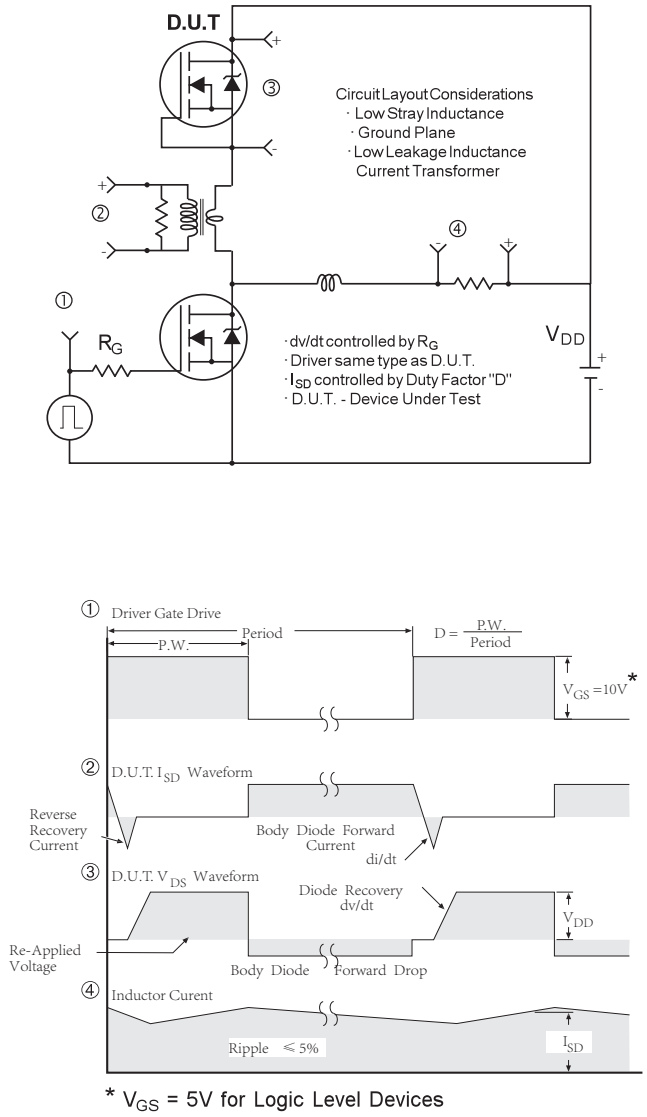
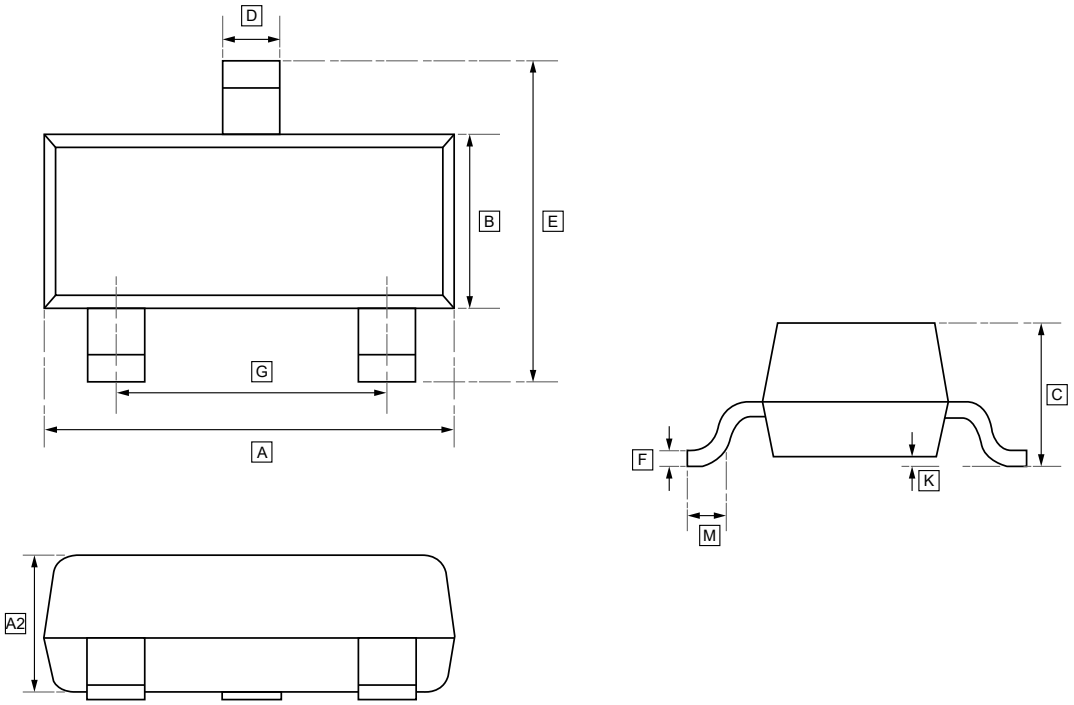


Fig 14. Fig13. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET ® Power Mosfets

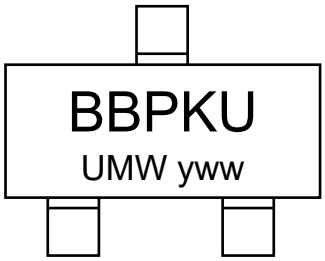
9.SOT-23 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	B	C	D	E	G	K	M	A2	F
Min	2.80	1.20	0.90	0.32	2.25	1.80	0.00	0.30	0.95	0.095
Max	3.04	1.40	1.10	0.55	2.55	2.00	0.10	-	1.05	0.115

10.Ordering information



yww: Batch Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRLML2803TR	SOT-23	3000	Tape and reel

11.Disclaimer

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