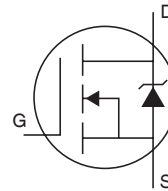
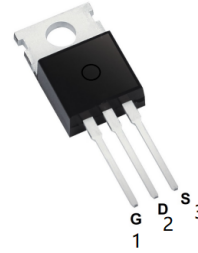


**Features**

- $V_{DS}(V) = 40V$
- $I_D = 75A$  ( $V_{GS} = 10V$ )
- $R_{DS(ON)} < 2.0m\Omega$  ( $V_{GS} = 10V$ )
- $R_{DS(ON)} < 2.3m\Omega$  ( $V_{GS} = 4.5V$ )



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	270	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (See Fig. 9)	190	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package Limited)	75	
$I_{DM}$	Pulsed Drain Current ①	1080	
$P_D @ T_C = 25^\circ C$	Maximum Power Dissipation	300	W
	Linear Derating Factor	2.0	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ②	540	mJ
$E_{AS} (tested)$	Single Pulse Avalanche Energy Tested Value ③	1160	
$I_{AR}$	Avalanche Current ①	See Fig.12a,12b,15,16	A
$E_{AR}$	Repetitive Avalanche Energy ④		mJ
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case		0.50⑤	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50		
$R_{\theta JA}$	Junction-to-Ambient		62	
$R_{\theta JA}$	Junction-to-Ambient (PCB Mount, steady state)⑥		40	

**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	40			V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient		0.031		V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance		1.5	2.0	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 75A ④
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance		1.8	2.3		V <sub>GS</sub> = 10V, I <sub>D</sub> = 75A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	2.0		4.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	130			S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 75A
I <sub>DSS</sub>	Drain-to-Source Leakage Current			20	μA	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V
				250		V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 125°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage			200	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage			-200		V <sub>GS</sub> = -20V
Q <sub>g</sub>	Total Gate Charge		160	240	nC	I <sub>D</sub> = 75A
Q <sub>gs</sub>	Gate-to-Source Charge		41	62		V <sub>DS</sub> = 32V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge		66	99		V <sub>GS</sub> = 10V ④
t <sub>d(on)</sub>	Turn-On Delay Time		13		ns	V <sub>DD</sub> = 20V
t <sub>r</sub>	Rise Time		120			I <sub>D</sub> = 75A
t <sub>d(off)</sub>	Turn-Off Delay Time		130			R <sub>G</sub> = 2.5Ω
t <sub>f</sub>	Fall Time		130			V <sub>GS</sub> = 10V ④
L <sub>D</sub>	Internal Drain Inductance		4.5		nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance		7.5			
C <sub>iss</sub>	Input Capacitance		6450		pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance		1690			V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance		840			f = 1.0MHz, See Fig. 5
C <sub>oss</sub>	Output Capacitance		5350			V <sub>GS</sub> = 0V, V <sub>DS</sub> = 1.0V, f = 1.0MHz
C <sub>oss</sub>	Output Capacitance		1520			V <sub>GS</sub> = 0V, V <sub>DS</sub> = 32V, f = 1.0MHz
C <sub>oss eff.</sub>	Effective Output Capacitance		2210			V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 32V
I <sub>S</sub>	Continuous Source Current (Body Diode)			270	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①			1080		
V <sub>SD</sub>	Diode Forward Voltage			1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 75A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time		56	84	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 75A, V <sub>DD</sub> = 20V
Q <sub>rr</sub>	Reverse Recovery Charge		67	100	nC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by T<sub>Jmax</sub>; starting T<sub>J</sub> = 25°C, L=0.24mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 75A, V<sub>GS</sub> = 10V. Part not recommended for use above this value.
- ③ I<sub>SD</sub> ≤ 75A, di/dt ≤ 220A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ④ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.
- ⑤ C<sub>oss eff.</sub> is a fixed capacitance that gives the same charging time as C<sub>oss</sub> while V<sub>DS</sub> is rising from 0 to 80% V<sub>DSS</sub>.
- ⑥ Limited by T<sub>Jmax</sub>, see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑦ This value determined from sample failure population. 100% tested to this value in production.
- ⑧ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑨ Max R<sub>DS(on)</sub> for D<sup>2</sup>Pak and TO-262 (SMD) devices.
- ⑩ TO-220 device will have an R<sub>th</sub> value of 0.45°C/W.

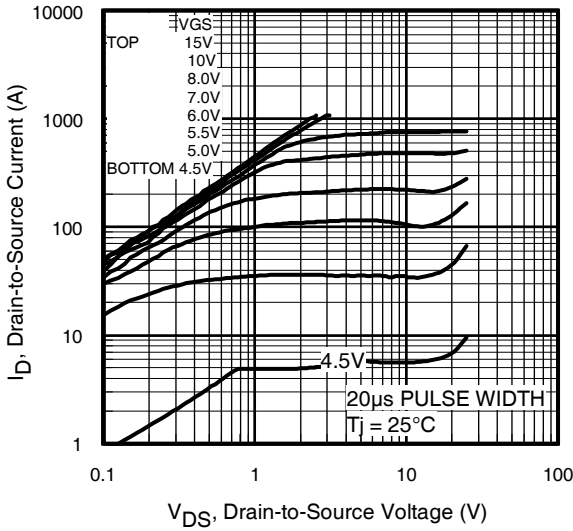


Fig 1. Typical Output Characteristics

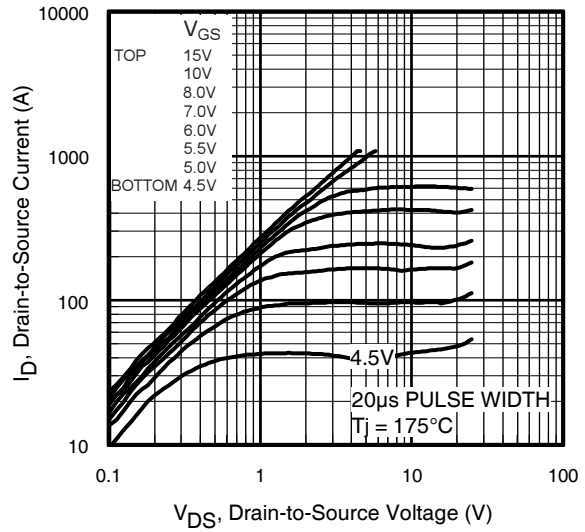


Fig 2. Typical Output Characteristics

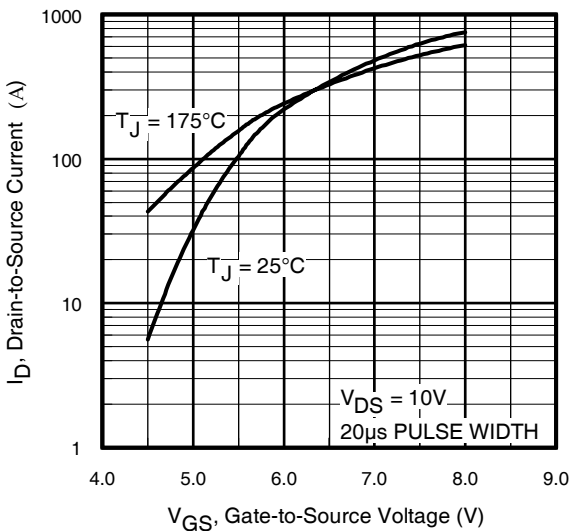


Fig 3. Typical Transfer Characteristics

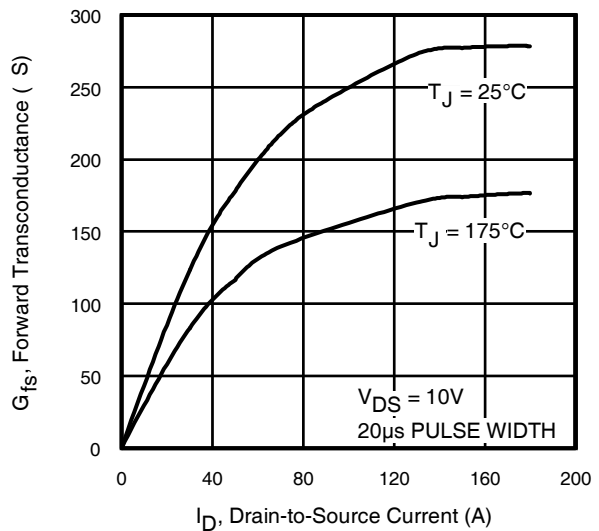


Fig 4. Typical Forward Transconductance vs. Drain Current

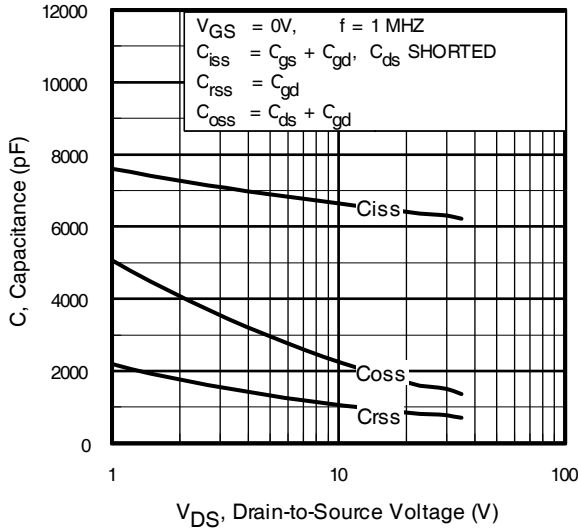


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

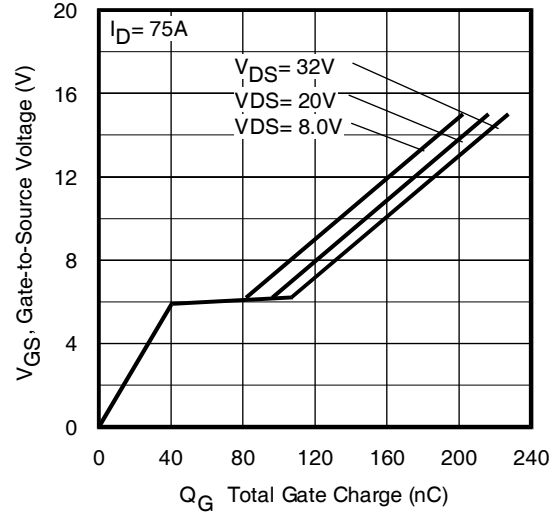


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

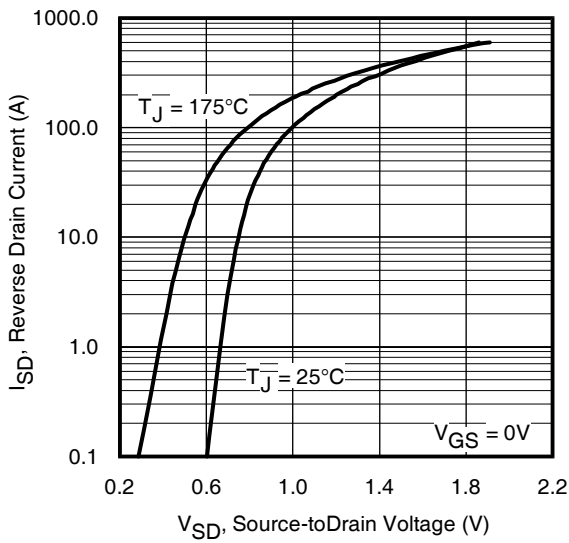


Fig 7. Typical Source-Drain Diode Forward Voltage

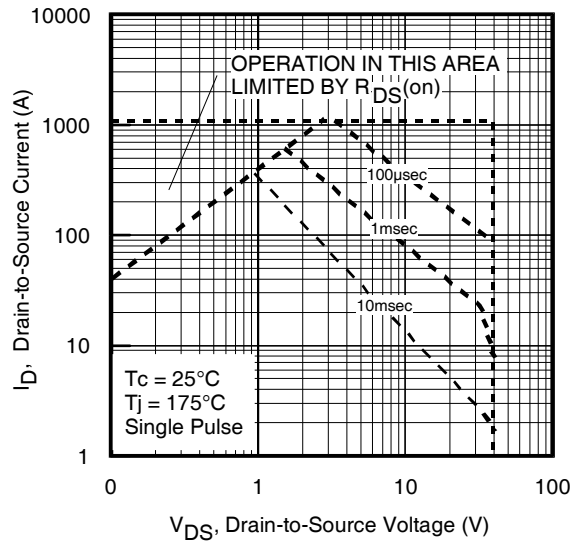


Fig 8. Maximum Safe Operating Area

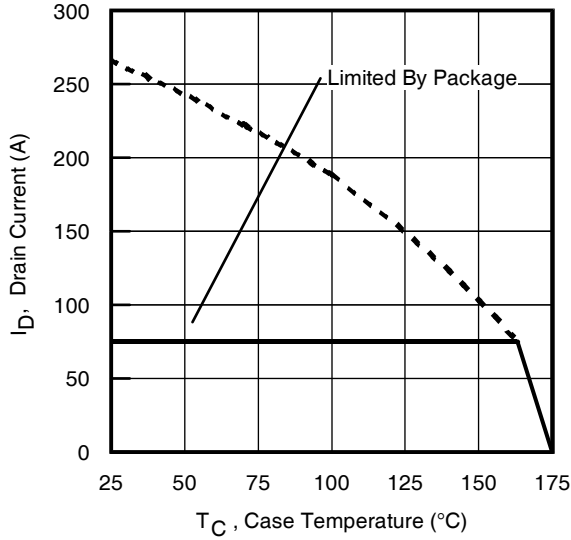


Fig 9. Maximum Drain Current vs. Case Temperature

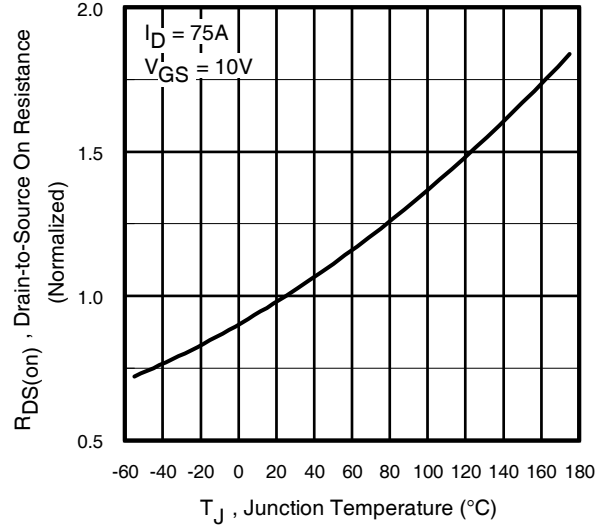


Fig 10. Normalized On-Resistance vs. Temperature

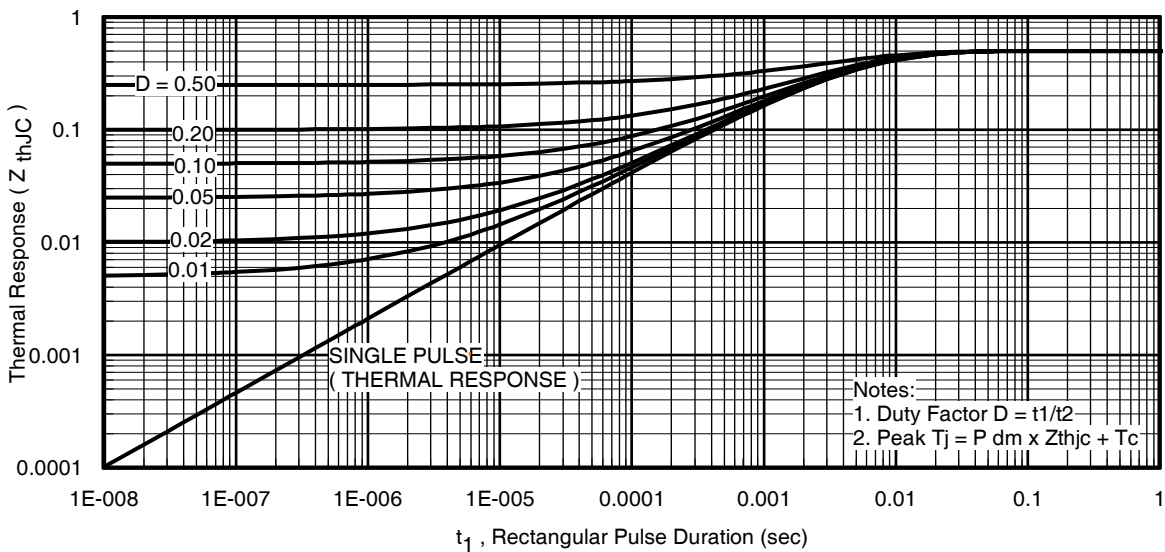


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

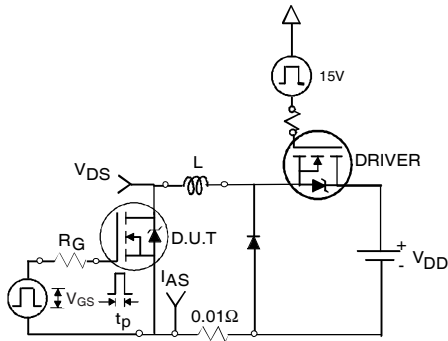


Fig 12a. Unclamped Inductive Test Circuit

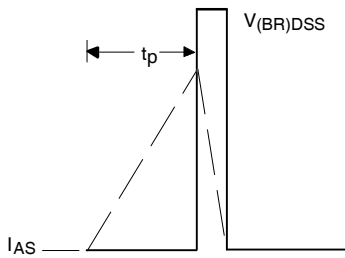


Fig 12b. Unclamped Inductive Waveforms

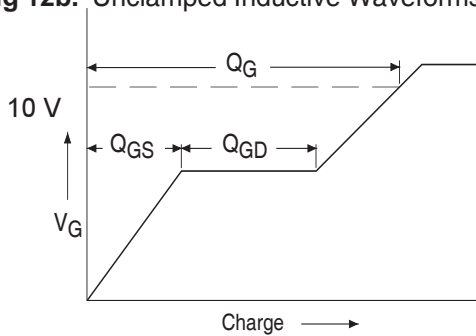


Fig 13a. Basic Gate Charge Waveform

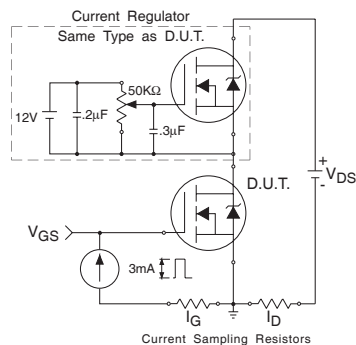


Fig 13b. Gate Charge Test Circuit

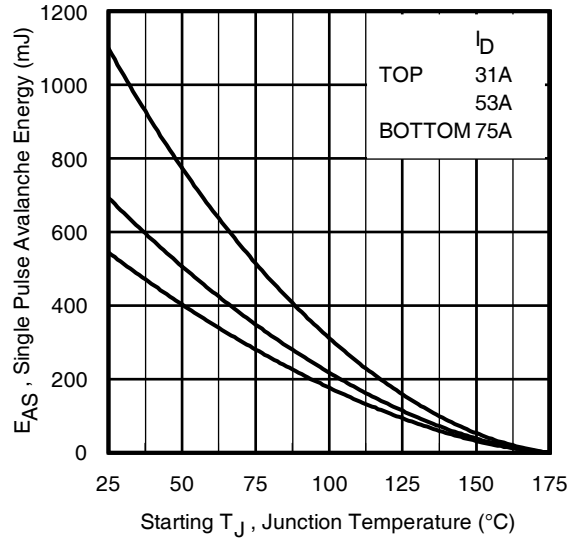


Fig 12c. Maximum Avalanche Energy vs. Drain Current

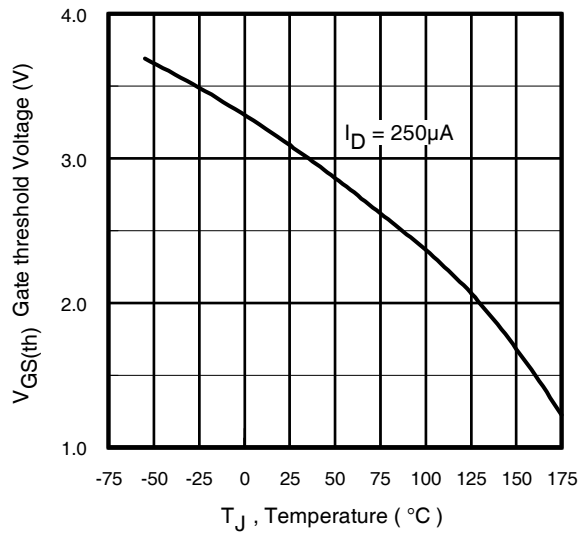


Fig 14. Threshold Voltage vs. Temperature

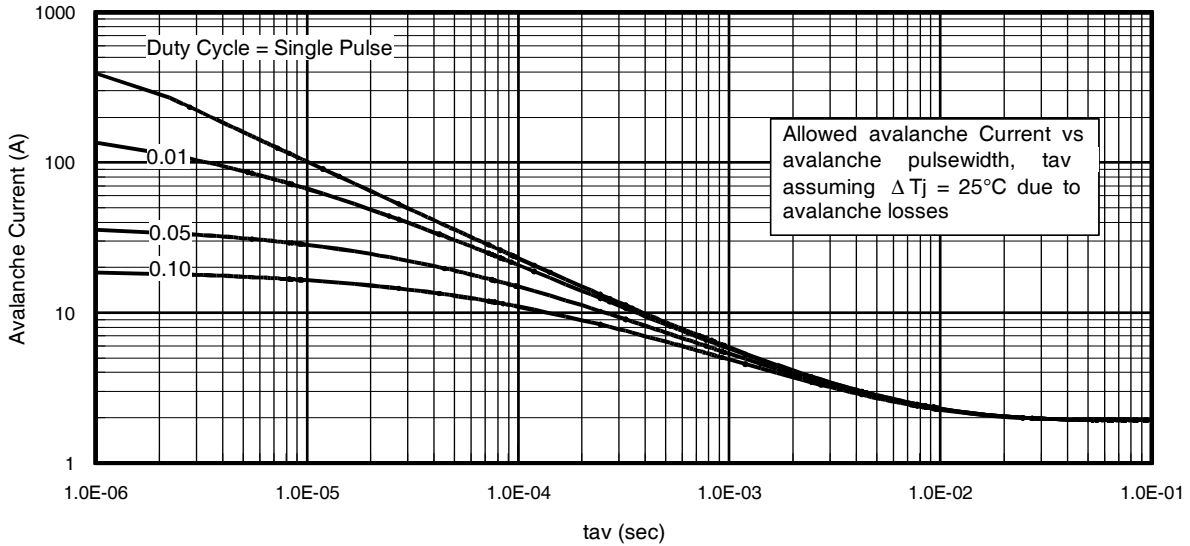


Fig 15. Typical Avalanche Current Vs.Pulswidth

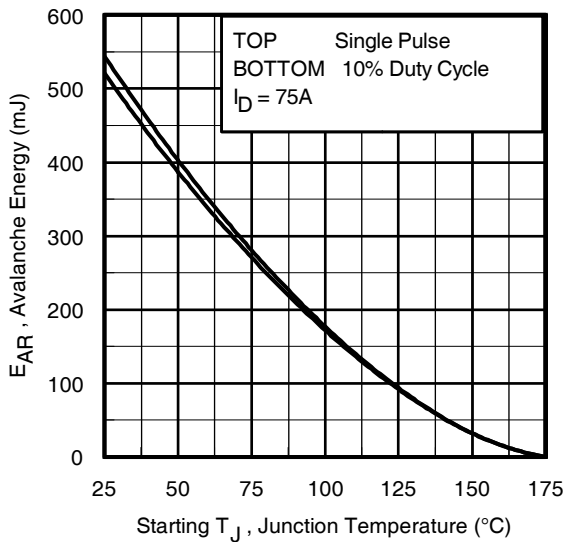


Fig 16. Maximum Avalanche Energy vs. Temperature

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

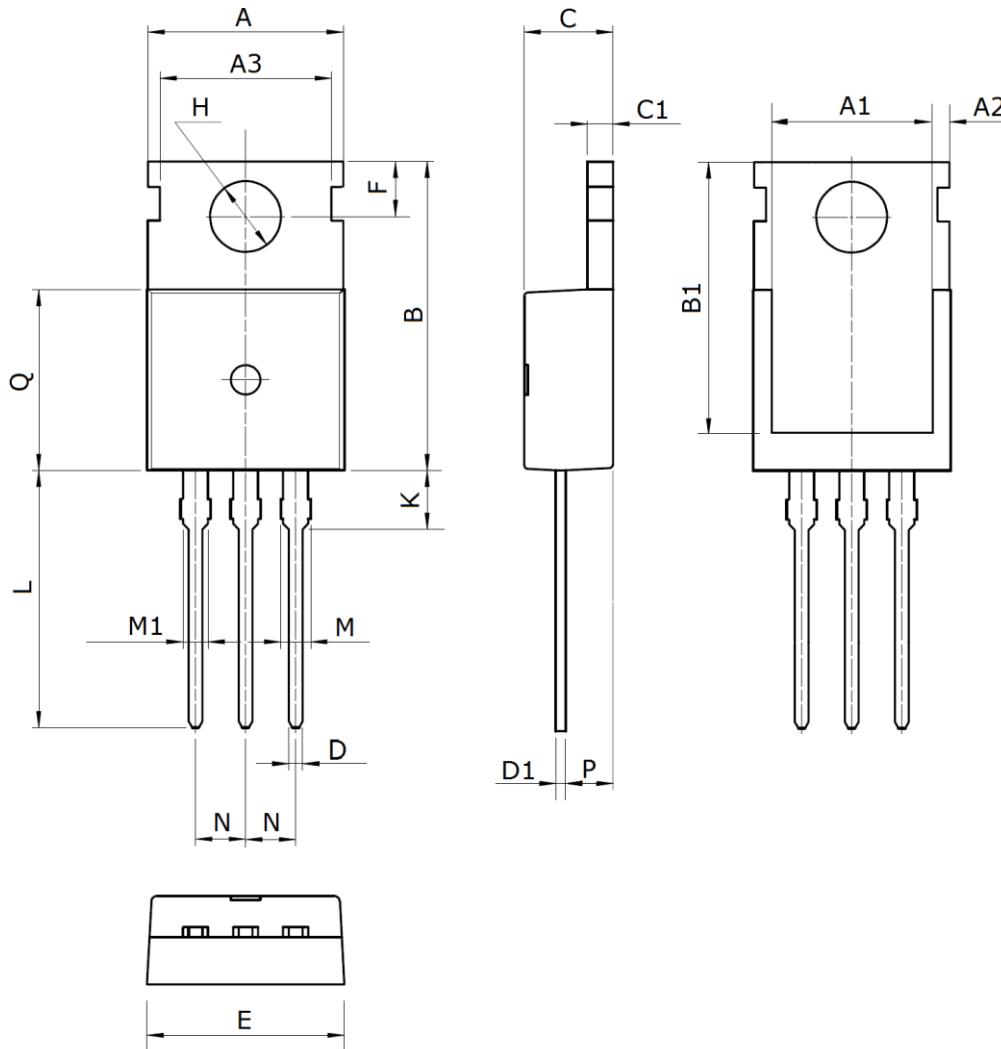
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Package Dimensions

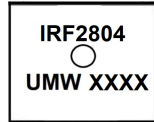
TO 220



Symbol	Dimensions (mm)	Symbol	Dimensions (mm)	Symbol	Dimensions (mm)
A	10.0±0.3	C1	1.3±0.2	L	13.2±0.4
A1	8.0±0.2	D	0.8±0.2	M	1.38±0.1
A2	0.94±0.1	D1	0.5±0.1	M1	1.28±0.1
A3	8.7±0.1	E	10.0±0.3	N	2.54(typ)
B	15.6±0.4	F	<b>2.8±0.1</b>	P	2.4±0.3
B1	<b>13.2±0.2</b>	H	3.6±0.1	Q	<b>9.15±0.25</b>
C	<b>4.5±0.2</b>	K	3.1±0.2		



**Marking**



**Ordering information**

Order code	Package	Baseqty	Deliverymode
UMW IRF2804PBF	TO-220	1000	Tube and box