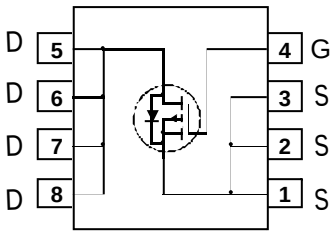
## General Description

This P-Channel MOSFET is a rugged gate version of advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gave drive voltage ratings (4.5V – 25V).




## Features

- $V_{DS\ (V)}$ = -30V
- $I_D$ = -5.3A($V_{GS}$ = -10V)
- $R_{DS(ON)}$ < 50mΩ ($V_{GS}$=-10V)
- $R_{DS(ON)}$ < 80mΩ ($V_{GS}$=-4.5V)
- Low gate charge
- Fast switching speed
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability

## Applications

- Power management
- Load switch
- Battery protection

## Absolute Maximum Ratings

$T_A$=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | –30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±25 | V |
| $I_D$ | Drain Current – Continuous | (Note 1a) | –5.3 | A |
| | – Pulsed | | –50 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 2.5 | W |
| | | (Note 1b) | 1.2 | |
| | | (Note 1c) | 1 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +175 | °C |

## Thermal Characteristics

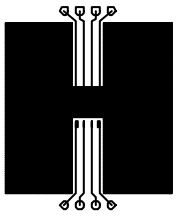
| | | | | |
|---|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 50 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction-to-Ambient | (Note 1c) | 125 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction-to-Case | (Note 1) | 25 | °C/W |

## Electrical Characteristics $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = –250 µA | –30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = –250 µA, Referenced to 25°C | | –23 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = –24 V, $V_{GS}$ = 0 V | | | –1 | µA |
| $I_{GSSF}$ | Gate–Body Leakage, Forward | $V_{GS}$ = 25 V, $V_{DS}$ = 0 V | | | 100 | nA |
| $I_{GSSR}$ | Gate–Body Leakage, Reverse | $V_{GS}$ = –25 V $V_{DS}$ = 0 V | | | –100 | nA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 µA | –1 | –1.7 | –3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = –250 µA, Referenced to 25°C | | 4.5 | | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = –10 V, $I_D$ = –5.3 A<br>$V_{GS}$ = –4.5 V, $I_D$ = –4 A | | 42<br>65 | 50<br>80 | mΩ |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS}$ = –10 V, $V_{DS}$ = –5 V | –25 | | | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = –5 V, $I_D$ = –5.3 A | | 10 | | S |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = –15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | | 528 | | pF |
| $C_{oss}$ | Output Capacitance | | | 132 | | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 70 | | pF |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = –15 V, $I_D$ = –1 A, $V_{GS}$ = –10 V, $R_{GEN}$ = 6 Ω | | 7 | 14 | ns |
| $t_r$ | Turn–On Rise Time | | | 13 | 24 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 14 | 25 | ns |
| $t_f$ | Turn–Off Fall Time | | | 9 | 17 | ns |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = –15 V, $I_D$ = –4 A, $V_{GS}$ = –10 V | | 10 | 14 | nC |
| $Q_{gs}$ | Gate–Source Charge | | | 2.2 | | nC |
| $Q_{gd}$ | Gate–Drain Charge | | | 2 | | nC |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | | | –2.1 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = –2.1 A (Note 2) | | –0.8 | –1.2 | V |

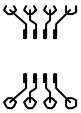
**Notes:**

**1.** $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1in² pad of 2 oz copper

b) 105°C/W when mounted on a .04 in² pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

**2.** Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

## Typical Characteristics

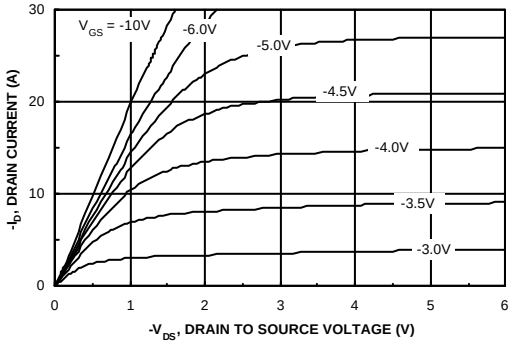



**Figure 1. On-Region Characteristics.**

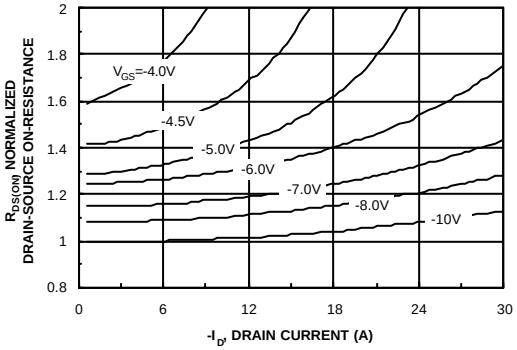



**Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.**

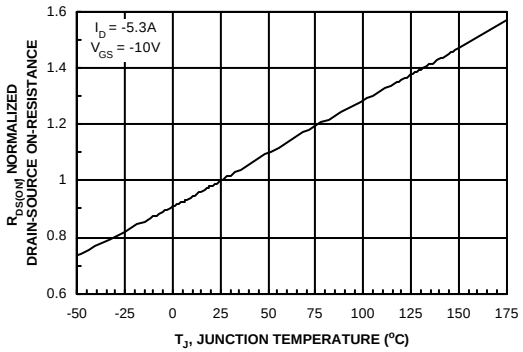



**Figure 3. On-Resistance Variation with Temperature.**

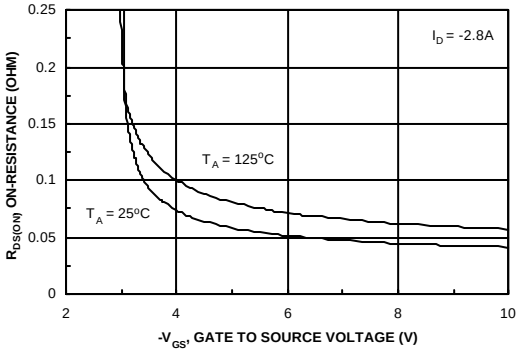



**Figure 4. On-Resistance Variation with Gate-to-Source Voltage.**

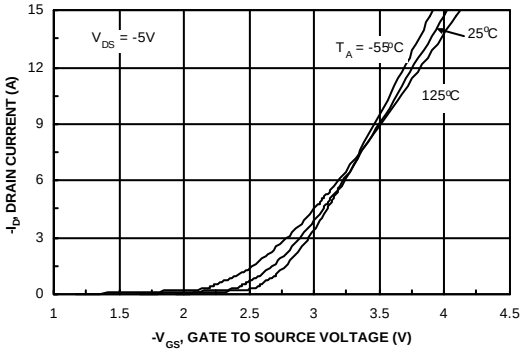



**Figure 5. Transfer Characteristics.**

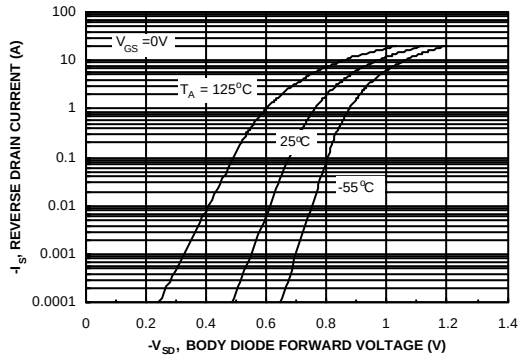



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.**

## Typical Characteristics

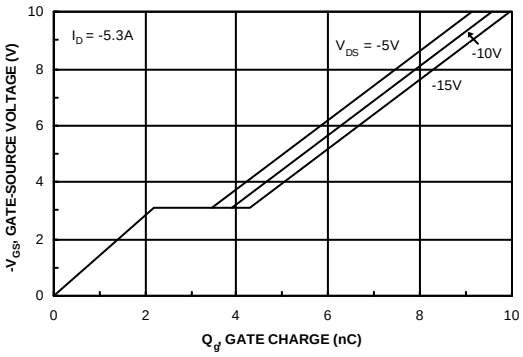



Figure 7. Gate Charge Characteristics.

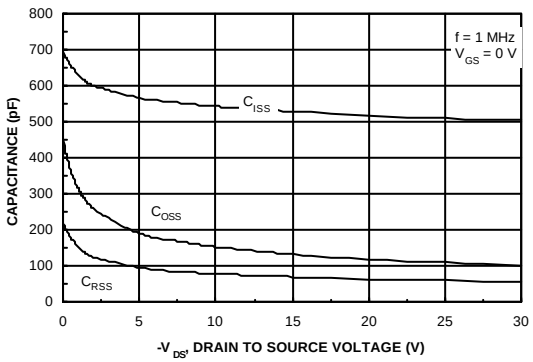



Figure 8. Capacitance Characteristics.

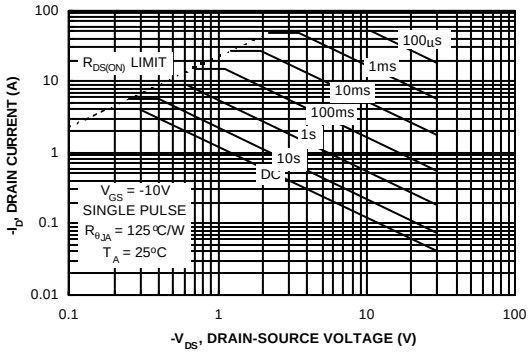



Figure 9. Maximum Safe Operating Area.

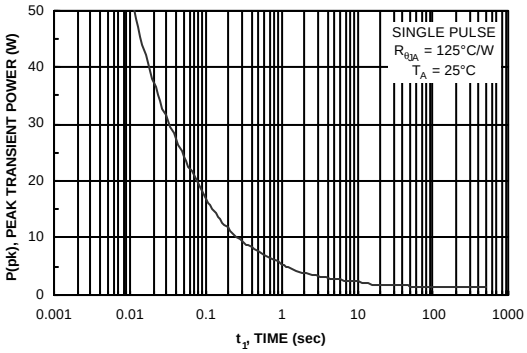



Figure 10. Single Pulse Maximum Power Dissipation.

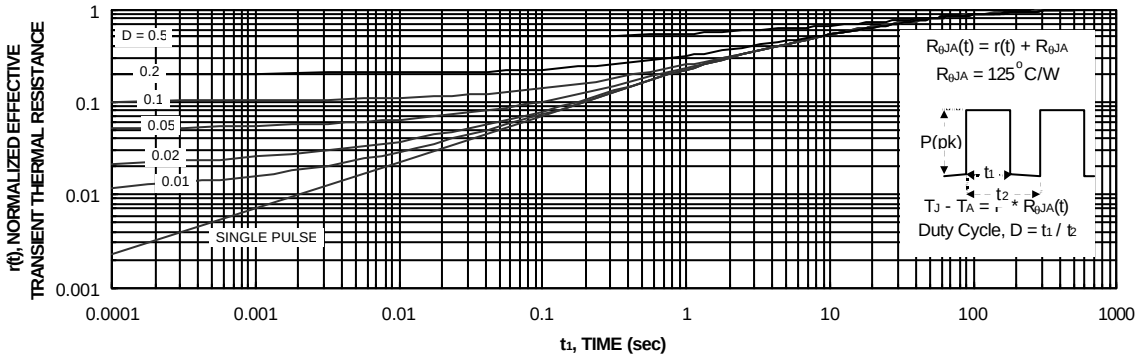
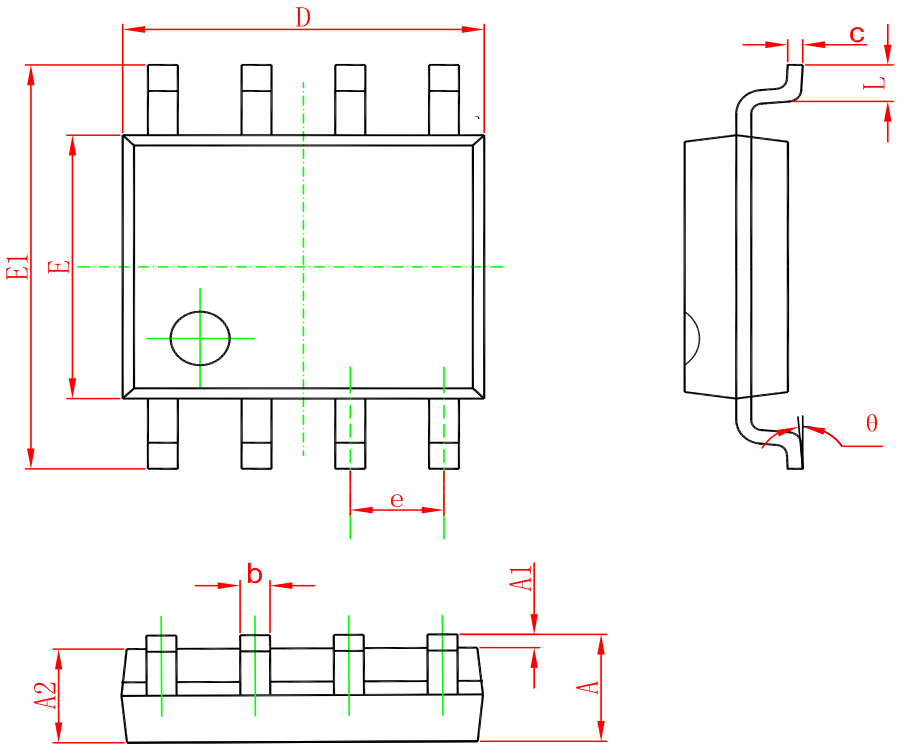



**Figure 11. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

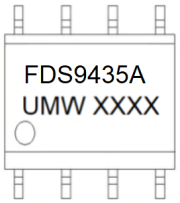
## PACKAGE OUTLINE DIMENSIONS

### SOP-8




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| A | 1.350 | 1.750 | 0.053 | 0.069 |
| A1 | 0.100 | 0.250 | 0.004 | 0.010 |
| A2 | 1.350 | 1.550 | 0.053 | 0.061 |
| b | 0.330 | 0.510 | 0.013 | 0.020 |
| c | 0.170 | 0.250 | 0.006 | 0.010 |
| D | 4.700 | 5.100 | 0.185 | 0.200 |
| E | 3.800 | 4.000 | 0.150 | 0.157 |
| E1 | 5.800 | 6.200 | 0.228 | 0.244 |
| e | 1.270(BSC) | | 0.050(BSC) | |
| L | 0.400 | 1.270 | 0.016 | 0.050 |
| θ | 0° | 8° | 0° | 8° |

## Marking




## Ordering information

| Order code | Package | Baseqty | Deliverymode |
|---|---|---|---|
| UMW FDS9435A | SOP-8 | 3000 | Tape and reel |