1.Description

UMW MAX31865 is an RTD-to-Digital converter that supports PT100 to PT1000 RTD inputs. MAX31865provides a precise external bias voltage via its BIAS pin and achieves accurate measurement by quantifying the ratio between the RTD and the Reference Resistor (RREF) connected in series to this bias voltage through the built-in ADC. UMW MAX31865 can provide noise rejection for 50Hz / 60Hz frequency based on the user's operating environment, minimizing the impact of external noise on measurement results. MAX31865supports 2-, 3-, and 4-wire RTD connections to accommodate different RTD measurement schemes. MAX31865 supports RTD fault detection and can identify various misconnections, including RTD open circuits, RTD short circuits, and RTD shorts to power supply or ground, facilitating users in quickly locating RTD faults.

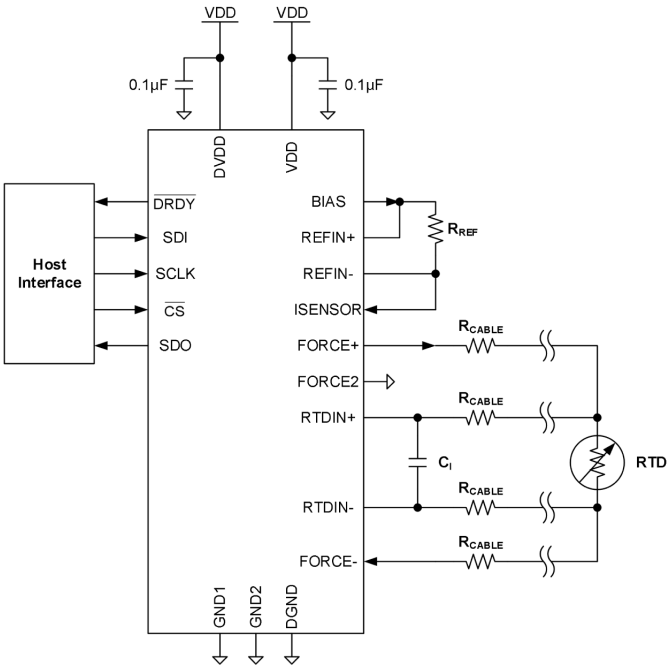
2.Features

- Chip operating temperature range: -55°C ~ +150°C
- Handles 100ohm to 1kohm (at 0°C) Platinum RTDs (PT100 to PT1000)
- Internal ADC resolution: 15bits
- Single measurement conversion Time:
  50Hz notch: 20.0ms
  60Hz notch: 16.7ms
- ADC Full-scale error: ±1LSB
- 50 / 60Hz noise rejection: 80dB
- Compatible with Mode 1/3 SPI interface
- Supports 2-wire, 3-wire, and 4-wire RTD connection
- Supply voltage range: 2.7V ~ 3.9V
- Supports RTD fault detection

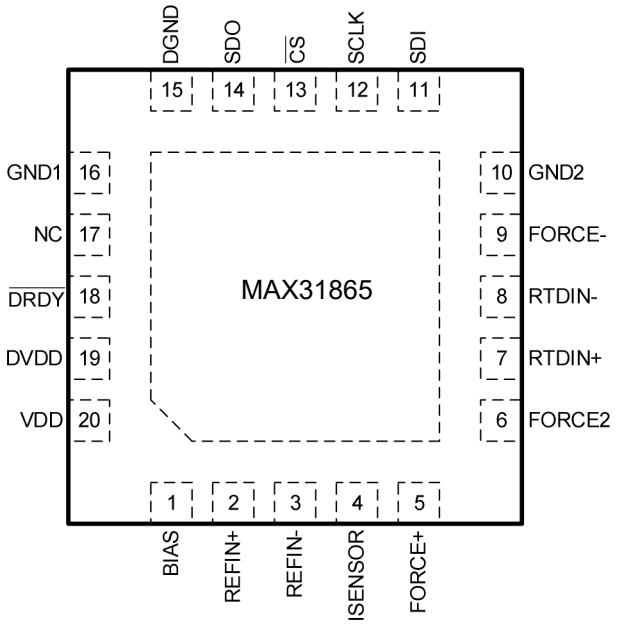
3.Applications

- Industrial Equipment
- Medical Equipment
- Instrumentation

4.MAX318654-Wire Connection Circuits



5.Pinning Information



QFN-20 Top View

Pin Function

Pin No	Pin Name	Description
1	BIAS	Bias voltage output (V_{BIAS}).
2	REFIN+	Positive reference voltage input. Connect to BIAS. Connect the RREF between REFIN+ and REFIN-.
3	REFIN-	Negative reference voltage input. Connect the RREF between REFIN+ and REFIN-.
4	ISENSOR	Low-Side of R_{REF}. Connect to REFIN-.
5	FORCE+	High-Side RTD drive. Connect to FORCE2 in 3-wire connection.
6	FORCE2	Positive input used in 3-Wire only. When in 3-wire connection, connect to FORCE+. When in 2-wire or 4-wire connection, connect to ground.
7	RTDIN+	Positive RTD input.
8	RTDIN-	Negative RTD input.
9	FORCE-	Low-Side RTD return.
10	GND2	Analog ground. Connect to GND1.
11	SDI	Serial-Data input in SPI interface.
12	SCLK	Serial-Clock input in SPI interface.
13	CS	Active-Low chip select. Set CS low to enable the SPI interface.
14	SDO	Serial-Data output in SPI interface.
15	DGND	Digital ground.
16	GND1	Analog ground. Connect to GND2.
17	NC	Do Not Connect.
18	DRDY	Low active Data-Ready pin. Push-pull output.
19	DVDD	Digital supply with 2.7V to 3.9V, bypass to DGND with a 0.1μF capacitor.
20	VDD	Analog supply with 2.7V to 3.9V, bypass to GND1 with a 0.1μF capacitor.

6.Absolute Maximum Ratings

Parameter	Min	Max	Units
VDD / DVDD	-0.3	6	V
Analog input/output pins	-0.3	VDD + 0.3	V
Digital input/output pins	-0.3	6	V
Operating temperature	-55	150	°C
Junction temperature		150	°C
Storage temperature	-60	160	°C

Unless otherwise noted, the specifications in the above table apply within the atmospheric temperature range. Stresses beyond the range may cause permanent damage to the device.

7.Electrostatic Protection

Parameter		Value	Units
Electrostatic Discharge Voltage	Human-body mode (HBM), per ANSI/ESDA/JEDEC JS-001-2017	±8000	V
	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002-2022	±1400	V
	Machine model (MM), per JESD22-A115C(2010)	±300	V
Latch-up effect	Latch-up (LU), per JESD 78F (2022)	±200	mA

8.Recommended Operating Conditions

Parameter	Min	Nom	Max	Units
Supply Voltage VDD / DVDD	2.7	3.3	3.9	V
Operating Temperature T_A	-50		150	°C
FORCE+ / FORCE2 / FORCE- / RTDIN+ / RTDIN-	0		V_{BIAS}	V
R_{REF}	350		10k	ohm
Cable resistance of RTD (per lead)	0		50	ohm

Unless otherwise noted, the specifications in the above table apply within the atmospheric temperature range.

9.Electrical Characteristics

Unless otherwise specified, the following data are the characteristics of the chip at T_A=-40°C ~ 125°C and VDD=3.0V ~ 3.6V; where TYP condition is T_A=27°C and VDD = 3.3V.

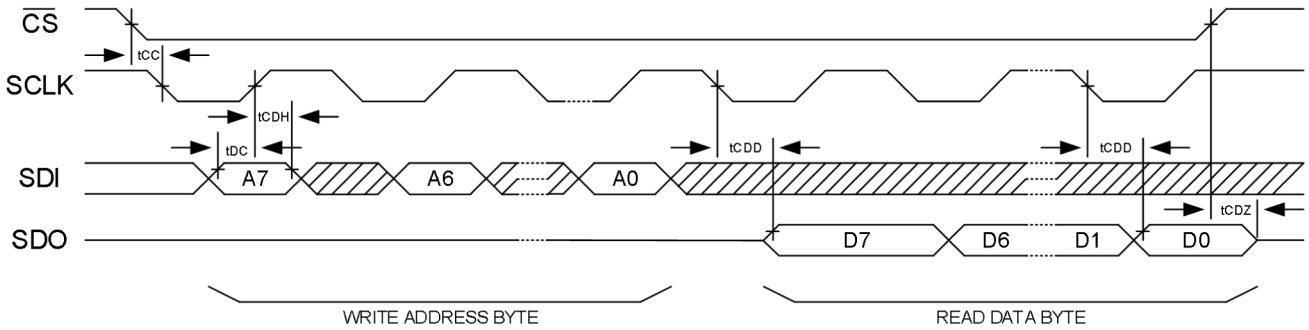
Parameter	Conditions	Min	Typ	Max	Units
Chip Operating Temperature Range		-50		150	°C
Internal ADC Resolution			15		bit
Input Leakage Current	RTDIN+ / RTDIN-			20	nA
Bias Voltage	V_{BIAS}	1.95	2	2.05	V
Bias Voltage Output Current	I_{OUT}	0.2		5.75	mA
Bias Voltage Load Regulation	I_{OUT}≤5.75mA		30		mV/mA
Bias Voltage Start-up Time	(Note 1)			10.5	ms
ADC Full-Scale Error			±1		LSB
ADC Offset Error				±3	LSB
50/60Hz Noise Rejection			80		dB
Common-Mode Rejection			90		dB
Conversion Time (Note 2)	Continuous conversion (60Hz notch)		16.7	18	ms
	Single conversion (60Hz notch)		52	56	ms
	Continuous conversion (50Hz notch)		20	21.5	ms
	Single conversion (50Hz notch)		62.5	67.5	ms
Auto Fault Detection Cycle Time	From CS high to cycle complete		550	600	µs
Power-Supply Rejection			±1		LSB/V
Quiescent Current	Active conversion		2	2.3	mA
	Shutdown mode		1	1.2	mA
Power-on and Power-off	Power-on reset		2.28		V
Reset Threshold	Power-on reset		2.16		V
Input Capacitance	Logic inputs		6		pF
Input Leakage Current	Logic inputs			±1	µA
Output High Voltage	Logic outputs, I_{OUT}=-1.6mA		DVDD -0.4		V
Output High Voltage	Logic outputs, I_{OUT}=1.6mA			0.4	V

Note 1: The maximum startup time of V_{BIAS} is determined by the RC delay formed by the 10kohm Reference Resistor and the 0.1μF bypass capacitor connected across the RTD.
Note 2: In continuous conversion mode, for 60Hz noise rejection, the initial conversion time is 52ms, and each subsequent conversion time is 16.7ms; for 50Hz noise rejection, the initial conversion time is 62.5ms, and each subsequent conversion time is 20ms.

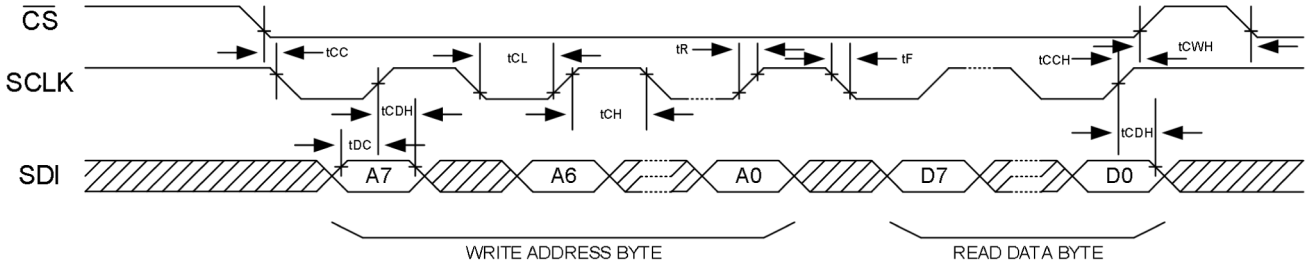
10.SPI Timing Requirements

Unless otherwise specified, the following data are the characteristics of the chip at T_A=-40°C ~ 125°C and VDD=3.0V ~ 3.6V.

Parameter	Symbol	Min	Typ	Max	Units
Data to SCLK Setup	t_{DC}	35			ns
SCLK to Data Hold	t_{CDH}	35			ns
SCLK to Data Valid	t_{CDD}			80	ns
SCLK Low Time	t_{CDL}	100			ns
SCLK High Time	t_{CDH}	100			ns
SCLK Frequency	t_{CLK}	DC		5	MHz
SCLK Rise and Fall	t_R, t_F			200	ns
$\overline{CS}$ to SCLK Setup	t_{CC}	400			ns
SCLK to $\overline{CS}$ Hold	t_{CCH}	100			ns
$\overline{CS}$ Inactive Time	t_{CWH}	400			ns
$\overline{CS}$ to Output High-Z	t_{CDZ}			40	ns
Address 01h or 02h Decoded to $\overline{DRDY}$ High	t_{DRDYH}		50		ns



NOTE:SCLK CAN BE EITHER POLARITY,TIMING SHOWN FOR CPOL=1



NOTE:SCLK CAN BE EITHER POLARITY,TIMING SHOWN FOR CPOL=1

11.Detailed Description

11.1 Device Functional Modes

11.1.1Overview of Temperature Measurement Based on RTD

RTDs measure temperature based on the principle that the resistance of a thermistor changes with temperature. The most common type of RTD employs platinum resistance (PT-RTD), which can measure temperatures exceeding 800°C and offers good accuracy, repeatability, and linearity.

For PT-RTDs, the most common models are PT100 and PT1000, with resistance values of 100 ohms and 1000 ohms at 0°C, respectively. For a PT100, the average slope α of its resistance between 0°C and 100°C depends on the impurities in the platinum and their concentrations. In the two most widely used standard protocols, α values are 0.00385 (IEC 751) and 0.00392 (SAMA), respectively. Therefore, the resistance of a PT100 is approximately linearly related to temperature, which can be specifically expressed by the Callendar-Van Dusen equation:

$$R(T) = R_0 * (1 + aT + bT^2 + c(T - 100)T^3)$$

In the above formula, T represents the temperature in degrees Celsius, R(T) is the resistance of the platinum at that temperature, and R0 is the resistance of the platinum at 0°C; taking the IEC 751 standard as an example, a = 3.90830 × 10^{-3}, b = -5.77500 × 10^{-7}, c = -4.18301 × 10^{-12} (-200°C ≤ T ≤ 0°C) / 0 (0°C ≤ T ≤ 850°C).

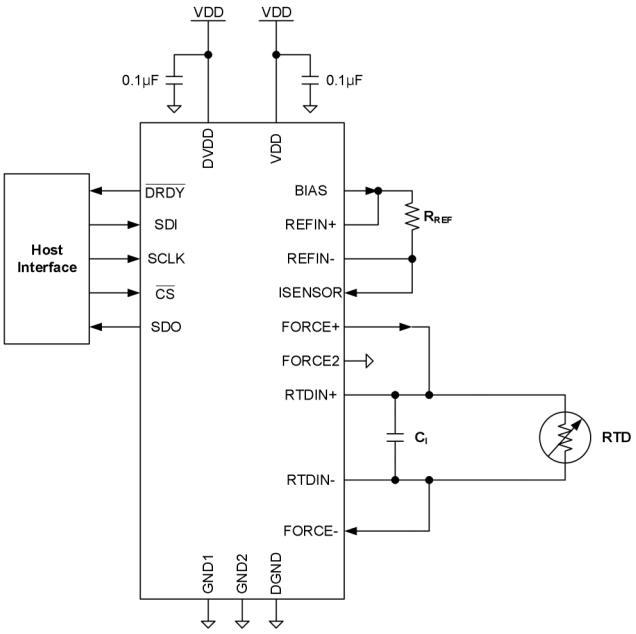


Figure 2: MAX318652-wire Connection Circuit

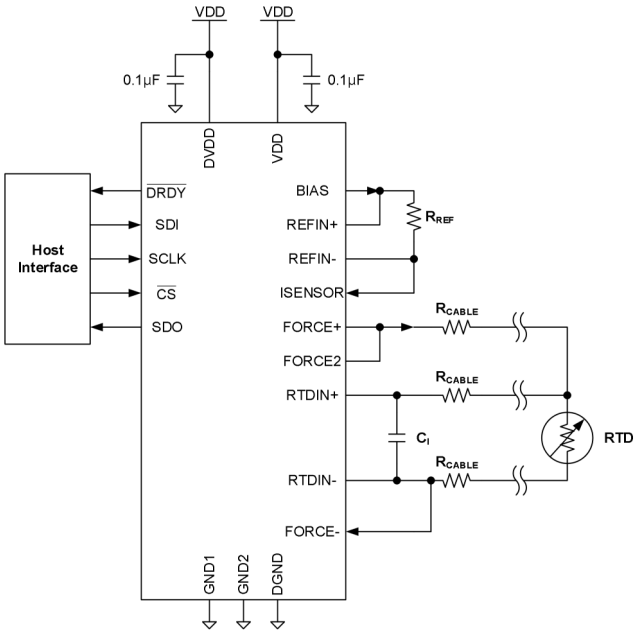


Figure 3: MAX318653-wire Connection Circuits

MAX31865 provides a precise and efficient solution for platinum resistance measurement. By connecting a reference resistor R_{REF} in series with the RTD under the BIAS pin of the MAX31865(as shown in Figure 1), the same current flows through both components. The value of the reference resistor R_{REF} is four times the value of the RTD at 0°C. Therefore, for a PT100, R_{REF} = 400ohms; for a PT1000, R_{REF} = 4000ohms. The voltage across the reference resistor R_{REF} serves as the quantization reference voltage for the internal ADC of the chip. MAX31865 uses this reference voltage to quantify the differential input voltage across the RTD, at which point the ADC's digital output represents the ratio between the RTD and RREF:

$$R_{RTD} = (ADC_Code * R_{REF}) / 2^{15}$$

For different usage scenarios, MAX31865 supports RTD connections in 2-, 3-, or 4-wire configurations. When the RTD is located close to the MAX31865, a 2-wire connection can be used (as shown in Figure 2); in this case, it should be noted that the resistance of the wires can cause errors in the final output, with a line resistance of 0.4ohms potentially resulting in a temperature error of approximately 1°C. A 4-wire connection (as shown in Figure 1) can be used to avoid this issue and enable long-distance remote temperature measurements, noting that the resistance of a single wire should be less than 50 ohms. In some scenarios, to reduce the number of wires connecting the remote RTD to the chip, a 3-wire connection can be employed (as shown in Figure 3). In this configuration, the FORCE2 pin of the MAX31865 should be connected to FORCE+. Writing a value of 1 to the 3-Wire bit (D4) in the Config register configures the MAX31865 to operate in 3-wire mode. After this configuration, the built-in ADC of the MAX31865 modifies its quantization method; if the wires are well-matched, the effect of the wire resistance can be automatically eliminated.

When using an RTD to measure temperatures in the range of -100°C to 100°C, the final temperature measurement value can be calculated according to the following formula:

$$\text{Temperature (°C)} = (\text{ADC code} / 32) - 256$$

The temperature measurement error of the above formula is -1.75°C at -100°C, 0°C at 0°C, and -1.4°C at 100°C (in the above results, it is assumed that the RTD used complies with the IEC 751 standard, and the value of R_{REF} is four times the resistance of the platinum RTD at 0°C). For higher accuracy, conversion can be performed using the Callendar-Van Dusen equation or by referring to the data in Table 1.

If the RTD used is not the PT100 or PT1000, MAX31865 can still be used in these cases, ensuring that the value of the R_{REF} is greater than or equal to the maximum value of the RTD within the temperature range of interest. At this time, the result of the ADC output is still the ratio of the RTD value to the R_{REF} value.

The table below shows the relationship between the actual temperature, RTD resistance, ADC output code, and measured temperature value when using PT100 with R_{REF} = 400ohms:

Temperature(°C)	RTD Resistance(ohm)	RTD Data Reg (01h–02h) (hex)	ADC Code (dec)	ADC Code/32-256(°C)
-200	18.52	0BDAh	1517	-208.59
-175	29.22	12B4h	2394	-181.19
-150	39.72	196Ch	3254	-154.31
-125	50.06	200Ah	4101	-127.84
-100	60.26	2690h	4936	-101.75
-75	70.33	2D04h	5762	-75.94
-50	80.31	3366h	6579	-50.41
-40	84.27	35EEh	6903	-40.28
-30	88.22	3876h	7227	-30.16
-20	92.16	3AFCh	7550	-20.06
-10	96.09	3D7Eh	7871	-10.03
0	100.00	4000h	8192	0.00
10	103.90	4280h	8512	10.00
20	107.79	44FCh	8830	19.94
30	111.67	4778h	9148	29.88
40	115.54	49F2h	9465	39.78
50	119.40	4C6Ah	9781	49.66
60	123.24	4EE0h	10096	59.50
70	127.08	5154h	10410	69.31
80	130.90	53C6h	10723	79.09
90	134.71	5636h	11035	88.84
100	138.51	58A4h	11346	98.56
110	142.29	5B12h	11657	108.28
120	146.07	5D7Ch	11966	117.94
130	149.83	5FE4h	12274	127.56
140	153.58	624Ch	12582	137.19
150	157.33	64B0h	12888	146.75

Temperature(°C)	RTD Resistance(ohm)	RTD Data Reg (01h–02h) (hex)	ADC Code (dec)	ADC Code/32-256(°C)
160	161.05	6714h	13194	156.31
170	164.77	6974h	13498	165.81
180	168.48	6BD4h	13802	175.31
190	172.17	6E30h	14104	184.75
200	175.86	708Ch	14406	194.19
225	185.01	7668h	15156	217.63
250	194.10	7C3Ah	15901	240.91
275	203.11	81FEh	16639	263.97
300	212.05	87B6h	17371	286.84
325	220.92	8D64h	18098	309.56
350	229.72	9304h	18818	332.06
375	238.44	989Ah	19533	354.41
400	247.09	9E24h	20242	376.56
425	255.67	A3A2h	20945	398.53
450	264.18	A914h	21642	420.31
475	272.61	AE7Ah	22333	441.91
500	280.98	B3D4h	23018	463.31
525	289.27	B922h	23697	484.53
550	297.49	BE64h	24370	505.56

11.1.2 Continuous Conversion Mode

The default power-on mode of the MAX31865 is the shutdown mode, during which its BIAS pin does not supply V_{BIAS} voltage, and the built-in ADC does not perform any conversions, leaving the chip in a low-power state. To enable the chip to enter continuous conversion mode, both the V_{BIAS} bit (D7) and the Conversion Mode bit (D6) of the Config register must be set to 1. Subsequently, the MAX31865 will initiate the corresponding continuous conversion according to the configurations of the 3-Wire bit (D4) and the 50/60Hz Filter Select bit (D0). Specifically, although the conversion times of the MAX31865 in continuous conversion mode are 16.7ms (D0=0, 60Hz notch) and 20ms (D0=1, 50Hz notch), the first conversion time after entering continuous conversion mode is 52ms (D0=0, 60Hz notch) and 62.5ms (D0=1, 50Hz notch).

11.1.3 One-Shot Mode

MAX31865 provides One-Shot mode. When the Conversion Mode bit (D6) of the Config register is set to 0 and the chip is in shutdown mode, writing 1 to the 1-Shot bit (D5) enables the MAX31865 to perform one single conversion. Before initiating a single conversion, if the V_{BIAS} bit (D7) has already been set to 1, writing 1 to the 1-Shot bit (D5) will start the single conversion immediately. If the V_{BIAS} bit (D7) is 0, it is necessary first to set the V_{BIAS} bit (D7) to 1 and wait at least 10.5ms for the RC network across the RTD to stabilize, and then write 1 to the 1-Shot bit (D5) to start the single conversion. The 1-Shot bit (D5) will automatically reset to 0 after the single conversion.

11.1.4 50/60Hz Noise Rejection

The 50/60Hz Filter Select bit (D0) of the MAX31865's Config register can switch the first notch frequency of the internal SINC3 filter, thereby suppressing noise at 50/60Hz and its higher-order harmonics, and improving the output accuracy of the chip. Please note, it is crucial not to change the 50/60Hz Filter Select bit (D0) during continuous conversion mode.

11.1.5 RTD Fault Detection

MAX31865 can detect various potential faults in RTDs. RTD fault detection can be divided into two types: 1) real-time automatic detection; 2) manual detection. For different RTD faults detection, the corresponding bits in the Fault Status register of the MAX31865 will be set to 1; the occurrence of any RTD fault will set bit D0 of the RTD LSB register to 1.

Real-time automatic detection includes the following checks:

1) After the chip powers on, it continuously monitors whether the voltages at the FORCE+, FORCE2, FORCE-, RTDIN+, and RTDIN- pins exceed the VDD voltage or fall below the GND1 voltage. If such a fault occurs, bit D2 of the Fault Status register will be set to 1, and the internal ADC of the MAX31865will stop conversions;

2) After the ADC completes each conversion, it determines whether the measured RTD resistance exceeds the value in the High Fault Threshold register or is below the value in the Low Fault Threshold register. If either condition occurs, bits D7/D6 of the Fault Status register will be set to 1; this check does not affect ADC conversions.

When performing manual detection with the MAX31865, it is possible to disconnect the switch that internally grounds the FORCE- pin to carry out the corresponding detection. Manual detection includes two modes: automatic delay mode and manual delay mode. When the establishment time of the RC network bridged across the RTD exceeds 100μs, the manual delay mode must be used. The above detection involves three voltage comparisons to determine the cause of faults, with the results returned to the Fault Status register:

1) Determine whether the voltage at the REFIN- pin is higher than 0.85 * V_{BIAS}; if it is, set bit D5 of the Fault Status register to 1;

2) Disconnect the switch that internally grounds the FORCE- pin, and determine whether the voltage at the REFIN- pin is lower than 0.85 * V_{BIAS}; if it is, set bit D4 of the Fault Status register to 1;

3) Keep the switch that internally grounds the FORCE- pin disconnected, and determine whether the voltage at the RTDIN- pin is lower than 0.85 * V_{BIAS}; if it is, set bit D3 of the Fault Status register to 1.

The three steps mentioned above need to be carried out in both the automatic delay mode and the manual delay mode. The difference lies in step 2), where after disconnecting the internal grounding switch of the FORCE- pin, the subsequent detection either proceeds automatically or waits for the host to send the corresponding command to continue. These actions are controlled by bits D3 and D2 in the Config register, as detailed in Table 2. Once the manually initiated detection is completed, the internal grounding switch of the FORCE- pin is reclosed, and bits D3 and D2 in the Config register are automatically reset to 0.

When manually initiating detection, it is necessary to ensure that bit D7 of the Config register is set to 1, and bits D6 and D5 are set to 0, meaning that the chip performs the above fault detection in the shutdown mode when V_{BIAS} stable. If bit D5 is set to 1 while configuring bits D3 and D2 in the Config register, all configurations will be ignored. If 100X100Xb is not written to the Config register in advance and 100X110Xb is written directly instead, the MAX31865 will start the detection in automatic delay mode.

Table 2 MAX31865 Fault-Detection Cycle Control Bits

D3	D2	Config Register Write	Write Action	Read Meaning
0	0	XXXX00XXb	/	Fault detection finished
0	1	100X010Xb	Fault detection with automatic delay	Automatic fault detection still running
1	0	100X100Xb	Run fault detection with manual delay (cycle 1)	Manual cycle 1 still running; waiting for user to write 11
1	1	100X110Xb	Finish fault detection with manual delay (cycle 2)	Manual cycle 2 still running

All the above RTD fault detection processes are shown in Figure 4, and Table 3 provides the correspondence between possible faults for different RTD connection methods and the Fault Status register values in such cases.

Writing a 1 to the Fault Status Clear bit (D1) of the MAX31865Config register, while ensuring that bits D5, D3, and D2 are all 0, can reset bits D7 to D2 of the Fault Status register and bit D0 of the RTD LSB register to 0. It should be noted that after being reset, bit D2 of the Fault Status register and bit D0 of the RTD LSB register may be immediately set to 1 again if the corresponding RTD fault is triggered.

After completing the clearing of the aforementioned flags, the Fault Status Clear bit will automatically reset to 0.

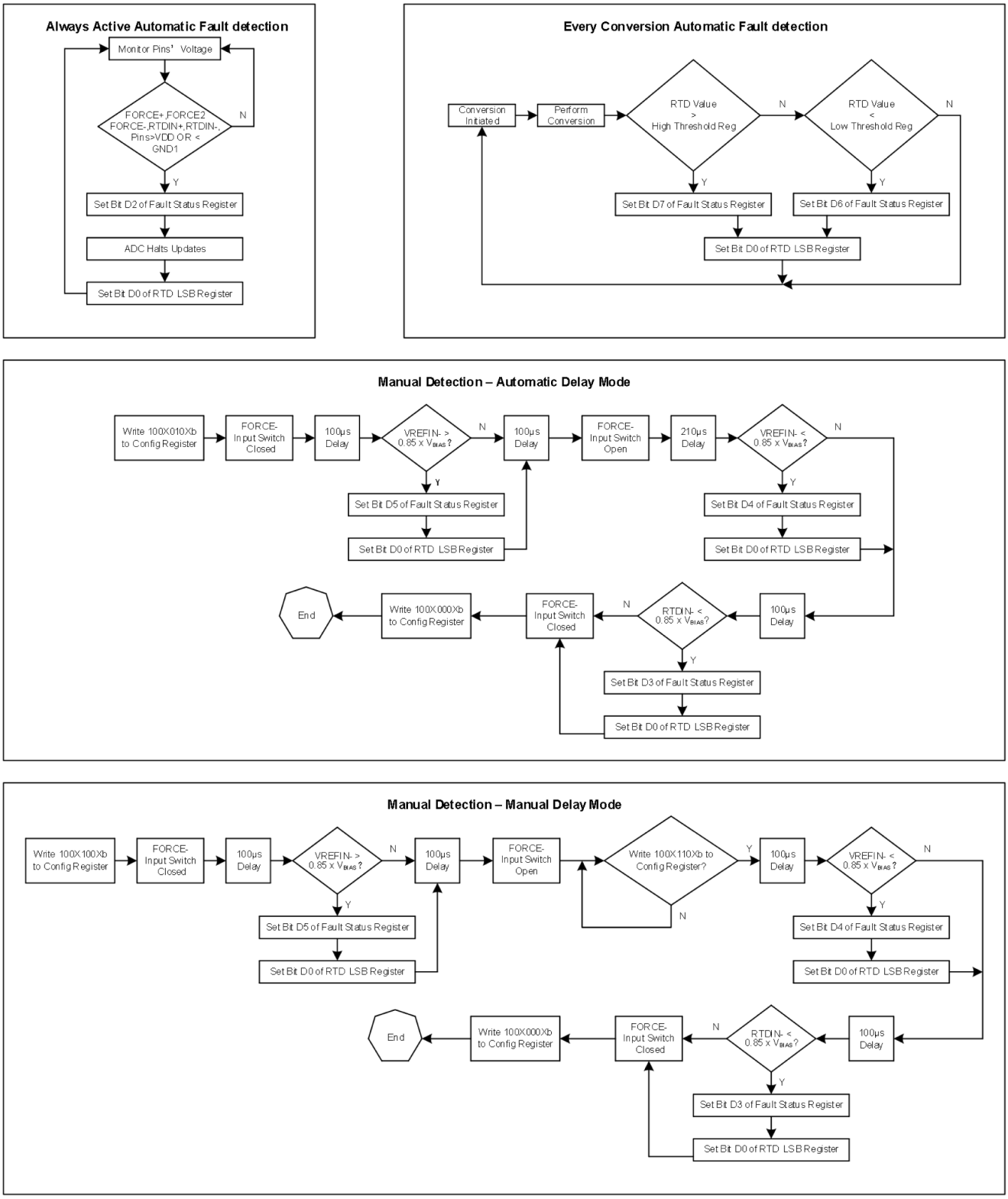


Figure 4: MAX31865 Fault Detection

Table 3 Summary of Faults in Different RTD Connection

Fault Status Reg	Possible Cause	Condition Detected	RTD Reg
2-Wire Connection			
D7	RTD Open	RTD Register > High Fault Threshold Register	FFFFh
D6	RTD Short	RTD Register< Low Fault Threshold Register	≈0000h
	RTDIN+ Short to GND		
D5	RTD Open	VREFIN- > 0.85 * V_{BIAS}	FFFFh
	RTDIN+ Short to VDD		Indeterminate
	RTDIN- Short to VDD		Indeterminate
D4	RTDIN- Short to GND	VREFIN- < 0.85 * V_{BIAS} (FORCE- Open)	Valid
D3	RTDIN- Short to GND	VRTDIN- < 0.85 * V_{BIAS} (FORCE- Open)	Valid
	RTDIN+ Short to GND		≈0000h
D2	>VDD / <GND1		Indeterminate
3-Wire Connection			
D7	RTD Open	RTD Register > High Fault Threshold Register	FFFFh
	RTDIN+ Short to VDD and Open with RTD		
	FORCE+ Short to VDD and Connect with RTD		
D6	RTDIN+ Short to RTDIN-	RTD Register < Low Fault Threshold Register	≈0000h
	RTDIN+ Short to GND and Open with RTD		
	FORCE+ Short to GND		
D5	RTD Open	VREFIN- > 0.85 * V_{BIAS}	FFFFh
	FORCE+ Short to VDD and Connect with RTD		
	FORCE+ Open		Indeterminate
	FORCE+ Short to VDD and Open with RTD		
	RTDIN- Short to VDD		

Fault Status Reg	Possible Cause	Condition Detected	RTD Reg
D4	RTDIN- Short to GND	VREFIN- < 0.85 * V_{BIAS} (FORCE- Open)	Valid
D3	FORCE+ Short to GND	VREFIN- < 0.85 * V_{BIAS} (FORCE- Open)	≈0000h
	RTDIN+ Short to GND and Connect with RTD		
	RTDIN- Short to GND		Valid
D2	>VDD/<GND1		Indeterminate
4-Wire Connection			
D7	RTD Open	RTD Register > High Fault Threshold Register	FFFFh
	RTDIN+ Short to VDD and Open with RTD		
	FORCE+ Short to VDD and Connect with RTD		
D6	RTDIN+ Short to RTDIN-	RTD Register < Low Fault Threshold Register	≈0000h
	RTDIN+ Short to GND and Open with RTD		
	RTDIN- Short to VDD and Open with RTD		
	FORCE+ Short to GND		

Fault Status Reg	Possible Cause	Condition Detected	RTD Reg
D5	RTD Open	VREFIN- > 0.85 * V_{BIAS}	FFFFh
	FORCE+ Short to VDD and Connect with RTD		
	FORCE+ Open		Indeterminate
	FORCE- Open		
	FORCE+ Short to VDD and Open with RTD		
	FORCE- Short to VDD and Open with RTD		
	FORCE-Short to VDD and Connect with RTD		
	FORCE- Short to GND and Open with RTD		
D4	FORCE-Short to GND and Connect with RTD	VREFIN- < 0.85 * V_{BIAS} (FORCE- Open)	Indeterminate
	RTDIN- Short to GND and Connect with RTD		Valid
D3	FORCE+ Short to GND	VRTDIN- < 0.85 * V_{BIAS} (FORCE- Open)	≈0000h
	RTDIN+ Short to GND and Connect with RTD		
	RTDIN- Short to GND and Connect with RTD		Valid
	FORCE- Short to GND		
D2	>VDD/<GND1		Indeterminate

11.1.6 $\overline{\text{DRDY}}$ Pin

The $\overline{\text{DRDY}}$ pin of the MAX31865will be pulled low after each update of the conversion results in the RTD register, indicating that the latest conversion results are available for reading. Once the read operation of the RTD register is completed, the $\overline{\text{DRDY}}$ pin will be pulled high again.

11.2 Serial Interface

11.2.1 Bus Overview

MAX31865 supports the Mode 1/3 SPI interface, that is, the SPI bus polarity CPOL = 0/1 and SPI bus phase CPHA = 1. The MAX31865 implements SPI communication using four pins: Serial Data Input (SDI), Serial Data Output (SDO), Serial Clock (SCLK), and Chip Select ($\overline{\text{CS}}$). The $\overline{\text{CS}}$ pin is active low, indicating the start and end of data transmission. The SCLK is generated by the host only when the $\overline{\text{CS}}$ pin is low.

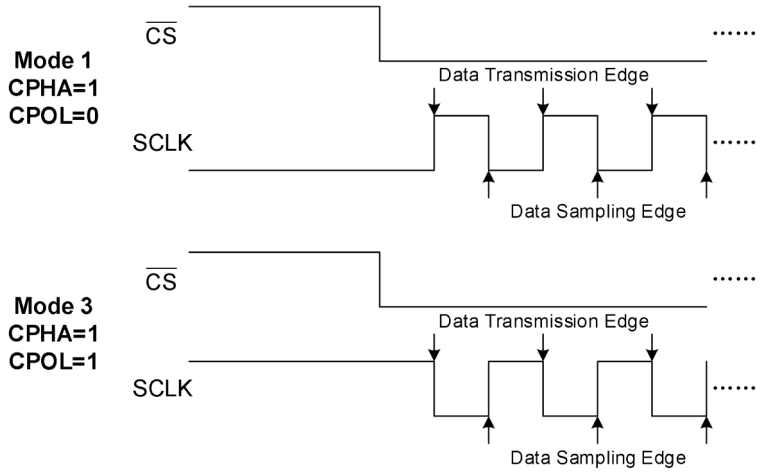


Figure 5: CPOL in Mode 1/3 SPI Interface

Figure 5 presents SCLK and CPOL in the Mode 1/3 SPI Interface. In Mode 1, CPOL = 0 and CPHA = 1; in this case, the initial value of SCLK is 0, the rising edge of SCLK is the data transmission edge, and the falling edge is the data sampling edge. In Mode 3, CPOL = 1 and CPHA = 1; in this case, the initial value of SCLK is 1, the falling edge of SCLK is the data transmission edge, and the rising edge is the data sampling edge. During SPI communication between the MAX31865 and the host computer, the MAX31865always samples the data written into the chip on the SDI line at the data sampling edge, and transmits the data to be read to the host computer via the SDO line at the data transmission edge. During SPI communication, both the addresses and data of MAX31865 are 8 bits, with the MSB transmitted first. The above process is detailed in Table 4

Table 4 Mode 1/3 SPI Interface Action

Mode	CSN	SCLK	SDI	SDO
Bus Idle	Bus Idle		Input Disabled	High impedance
Write	Low	CPOL = 0, SCLK Falling	Data Bit Latch	High impedance
		CPOL = 1, SCLK Rising		
Read	Low	CPOL = 0, SCLK Rising	X	Next data bit shift
		CPOL = 1, SCLK Falling		

11.2.2 Read and Write Operations

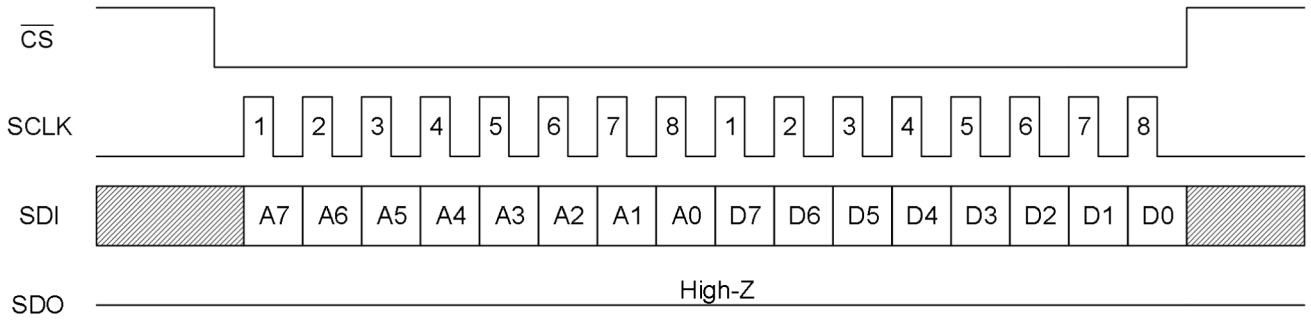


Figure 6: Single Byte Write Operation

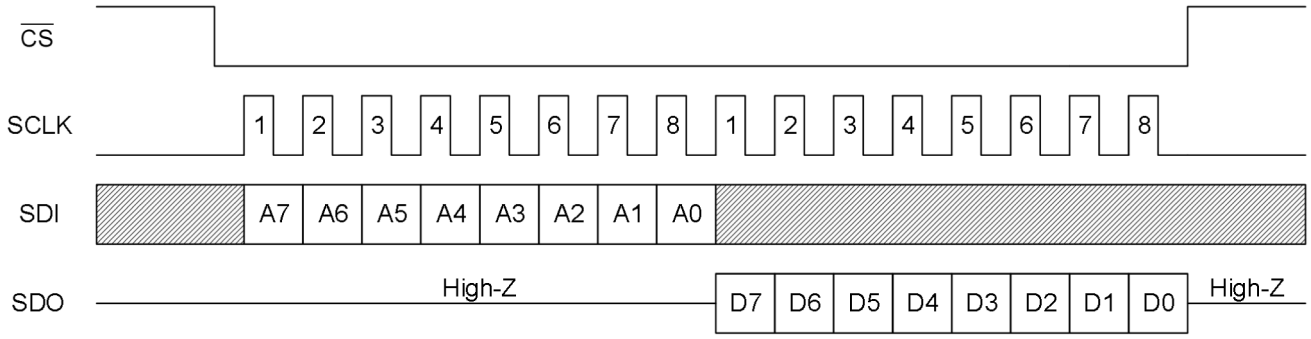


Figure 7: Single Byte Read Operation

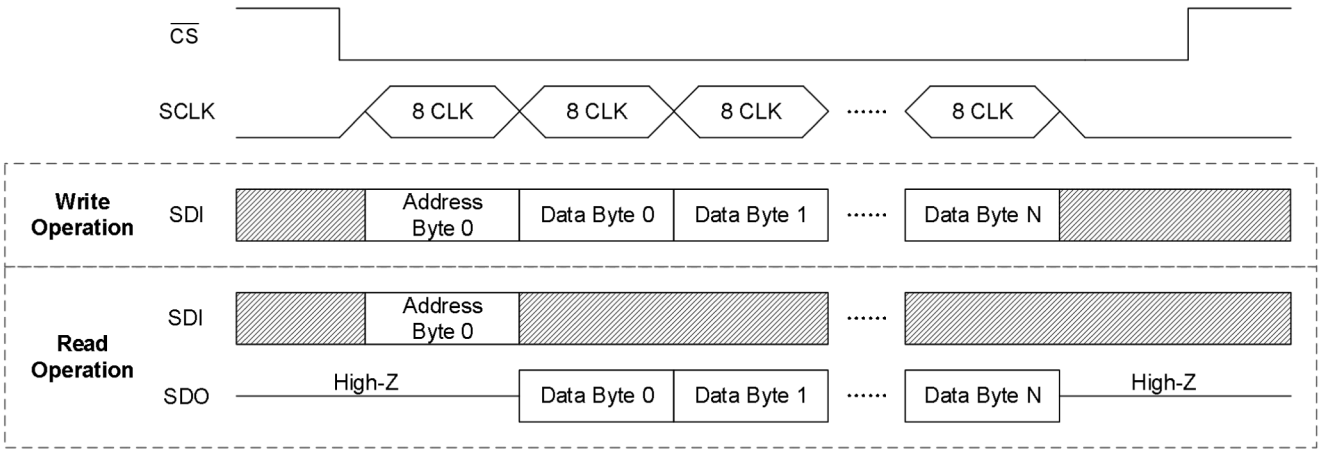


Figure 8: Multiple Bytes Write and Read Operation

During SPI communication between the MAX31865 and the host computer, both the address and data bytes are shifted into the serial data input line (SDI) in MSB-first order to perform write operations, and shifted out from the serial data output line (SDO) to complete read operations. During communication, after $\overline{CS}$ pulling low, the address byte must be sent first, with the most significant bit of the address byte indicating whether the subsequent data will be written or read, followed by one or more data bytes. If the most significant bit of the address byte is 1, it indicates that the following bytes are write data; if the most significant bit is 0, it indicates that the following bytes are read data.

MAX31865 supports single-byte or multi-byte read and write operations. For single-byte read/write operations, after $\overline{CS}$ pulling low, the bus begins transmitting the address byte and 1 byte of data, and then $\overline{CS}$ pulling high ends this communication (see Figure 6 and Figure 7). After transmitting 1 byte of data, the host can keep pulling $\overline{CS}$ low and send SCLK, allowing the chip to continue multi-byte read/write operations. The address byte corresponding to the subsequent data bytes will automatically increment (see Figure 8). When the address byte increments to 7Fh / FFh, it will automatically wrap around to 00h / 80h. Data read from registers not defined in Table 5 will return FFh; writing to read-only registers will not change their values.

11.3 Register Description

Table 5 provides the read and write addresses as well as the power-on initial values of the internal registers of the MAX31865. All registers within the MAX31865have a bit width of 8 bits.

Table 5 MAX31865 Internal Registers

Register Name	Read Address	Write Address	POR Value	Type
Configuration	00h	80h	00h	R/W
RTD MSB	01h	/	00h	R
RTD LSB	02h	/	00h	R
High Fault Threshold MSB	03h	83h	FFh	R/W
High Fault Threshold LSB	04h	84h	FFh	R/W
Low Fault Threshold MSB	05h	85h	00h	R/W
Low Fault Threshold LSB	06h	86h	00h	R/W
Fault Status	07h	/	00h	R

11.3.1 Configuration Register

Table 6 Configuration Register Description

Bit	Bit	Description	POR Value
D7	V_{BIAS}	0=V_{BIAS} Disabled; 1=V_{BIAS} Enabled;	0
D6	Conversion Mode	0=Shutdown Mode; 1=Continuous Conversion Mode;	0
D5	1-Shot	1=One-Shot Mode when D7=1 / D6=0; This bit can automatically reset to 0;	0
D4	3-Wire	0=2/4 Wire Connection; 1=3 Wire Connection;	0
D3:D2	Fault Detection Control	See Details in Table 2;	00
D1	Fault Status Clear	1= The D7:D2 bits in the Fault Status register and the D0 bit in the RTD LSB register are reset to 0; This bits can automatically reset to 0;	0
D0	50/60Hz Filter Select	0=60Hz Noise Rejection; 0=50Hz Noise Rejection;	00

For detailed usage of each bit in the table, please refer to Section 7.1.

11.3.2 RTD Register / Fault Threshold Register

Table 7 RTD Register / Fault Threshold Register Description

	RTD MSB Register (01h)								RTD LSB Register (02h)							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	Fault
	High Fault Threshold MSB Register (04h)								**High Fault Threshold LSB Register (04h)**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit	H14	H13	H12	H11	H10	H9	H8	H7	H6	H5	H4	H3	H2	H1	H0	/
	Low Fault Threshold MSB Register (05h)								**Low Fault Threshold LSB Register (06h)**							
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Bit	L14	L13	L12	L11	L10	L9	L8	L7	L6	L5	L4	L3	L2	L1	L0	/

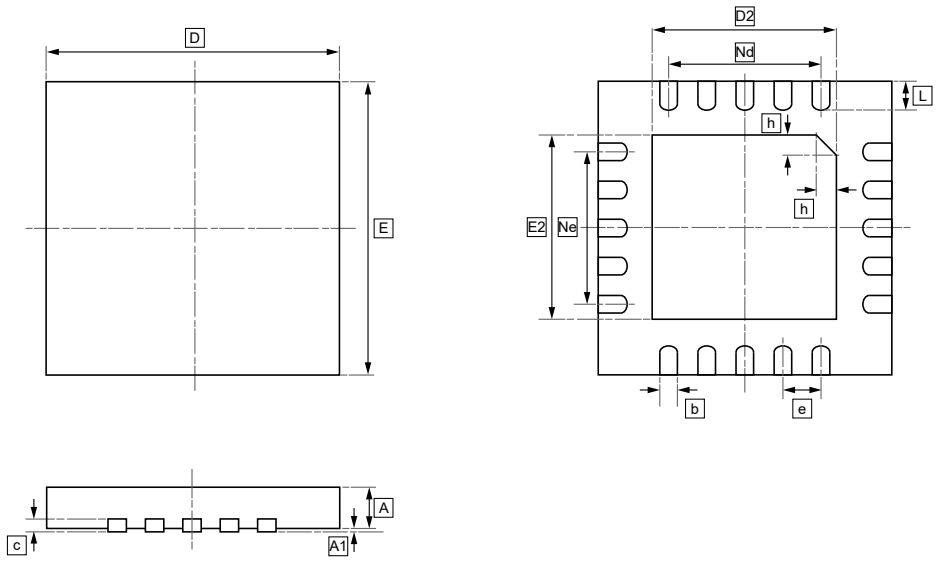
The RTD Register, High Fault Threshold Register, and Low Fault Threshold Register of the MAX31865 share the same data format. The power-on initial value of the High Fault Threshold Register is FFFFh, while the power-on initial value of the Low Fault Threshold Register is 0000h.

11.3.3 Fault Status Register

Table 8 Fault Status Register Description

Bit	Bit Name	Description of Bit = 1	POR Value
D7	RTD High Threshold	RTD measurement value > High Fault Threshold Register;	0
D6	RTD Low Threshold	RTD measurement value < Low Fault Threshold Register;	0
D5	REFIN- > 0.85 * V_{BIAS}	See details in Section 7.1.5;	0
D4	REFIN- < 0.85 * V_{BIAS} (FORCE- Open)		0
D3	RTDIN- < 0.85 * V_{BIAS} (FORCE- Open)		0
D2	Overvoltage/ Undervoltage Fault	FORCE+ / FORCE2 / FORCE- / RTDIN+ / RTDIN-Pin Voltage > VDD / < GND1;	0
D1:D0	/	/	00

12.QFN-20 Package Outline Dimensions

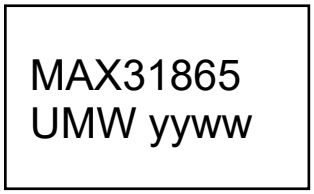


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	b	c	D	D2	e	Ne	Nd	E	E2	L
Min	0.70	-	0.25	0.18	4.90	3.05	0.65	2.60	2.60	4.90	3.05	0.45
Max	0.80	0.05	0.35	0.25	5.10	3.25	BSC	BSC	BSC	5.10	3.25	0.65

Symbol	h
Min	0.30
Max	0.40

13.Ordering Information



yy: Year Code
ww: Week Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW MAX31865AAP+T	MAX31865	SSOP-20-208mil	2000	Tape and reel
UMW MAX31865ATP+T	MAX31865	QFN-20-EP(5x5)	4000	Tape and reel

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