UMW AO4832

30V Dual N-Channel MOSFET

1.Description

The AO4832 uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge.This device is suitable for high side switch in SMPS and g eneral purpose applications.

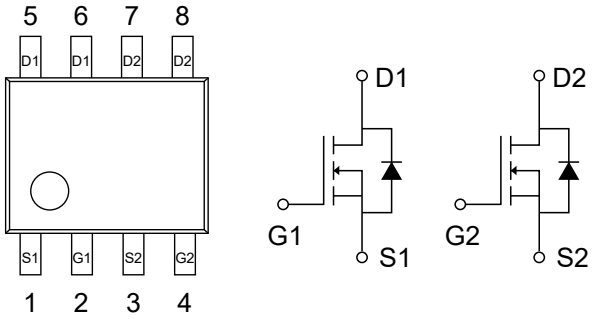
2.Features

- $V_{DS\ (V)}$=30V
- I_D=10A(V_{GS}=10V)
- $R_{DS(ON)}$<13mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<17.5mΩ(V_{GS}=4.5V)

3.Pinning information

Pin	Symbol	Description
2,4	G1, G2	GATE
1,3	S1, S2	SOURCE
5,6,7,8	D1, D2	DRAIN

SOP-8



4.Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Rating	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	
Continuous Drain Current	T_A=25°C	I_D	10	A
	T_A=70°C		8	
Pulsed Drain Current [c]		I_{DM}	55	
Avalanche Current [c]		I_{AS}, I_{AR}	22	
Avalanche energy L=0.1mH [c]		E_{AS}, E_{AR}	24	mJ
Power Dissipation [B]	T_A=25°C	P_D	2	W
	T_A=70°C		1.3	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

5.Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	48	62.5	°C/W
Maximum Junction-to-Ambient [A D]	Steady-State		74	90	°C/W
Maximum Junction-to-Lead	Steady-State	$R_{\theta JL}$	32	40	°C/W

6.Electrical Characteristics (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	30			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=30V, V_{GS}=0V			1	μA
		T_J=55°C			5	
Gate-Body leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±20V			100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1.5	1.9	2.5	V
On state drain current	$I_{D(ON)}$	V_{GS}=10V, V_{DS}=5V	55			A
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=10A		10.8	13	mΩ
		V_{GS}=4.5V, I_D=8A		14	17.5	mΩ
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=10A		43		S
Diode Forward Voltage	V_{SD}	I_S=1A, V_{GS}=0V		0.75	1	V
Maximum Body-Diode Continuous Current	I_S				2.5	A
DYNAMIC PARAMETERS						
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=15V, f=1MHz	610	760	910	pF
Output Capacitance	C_{oss}		88	125	160	pF
Reverse Transfer Capacitance	C_{rss}		40	70	100	pF
Gate resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz	0.8	1.6	2.4	Ω
SWITCHING PARAMETERS						
Total Gate Charge	Q_g(10V)	V_{GS}=10V, V_{DS}=15V, I_D=10A	11	14	17	nC
Total Gate Charge	Q_g(4.5V)		5	6.6	8	nC
Gate Source Charge	Q_{gs}			2.4		nC
Gate Drain Charge	Q_{gd}			3		nC
Turn-On DelayTime	$t_{D(on)}$	V_{GS}=10V, V_{DS}=15V, R_L=1.5Ω,R_{GEN}=3Ω		4.4		ns
Turn-On Rise Time	t_r			9		ns
Turn-Off DelayTime	$t_{D(off)}$			17		ns
Turn-Off Fall Time	t_f			6		ns
Body Diode Reverse Recovery Time	t_{rr}	I_F=10A, dI/dt=500A/μs	5.6	7	8	ns
Body Diode Reverse Recovery Charge	Q_{rr}	I_F=10A, dI/dt=500A/μs	6.4	8	9.6	nC

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in ^{2} FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on $T_{J(MAX)}$=150°C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedence which is measured with the device mounted on 1 in ^{2} FR-4 board with 2oz. Copper, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C. The SOA curve provides a single pulse rating.

7.1TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

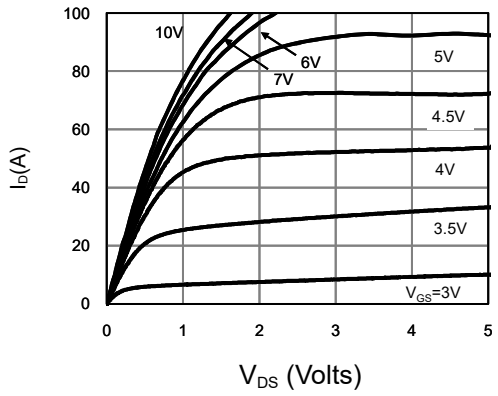


Fig 1: On-Region Characteristics (Note E)

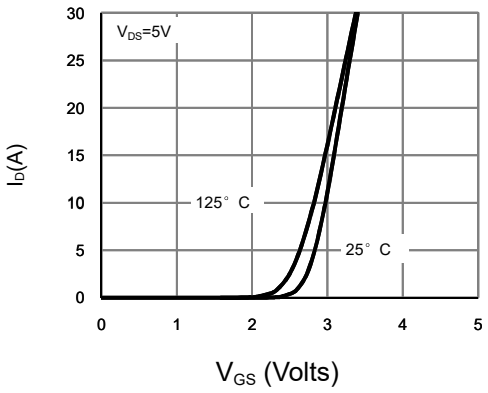


Figure 2: Transfer Characteristics (Note E)

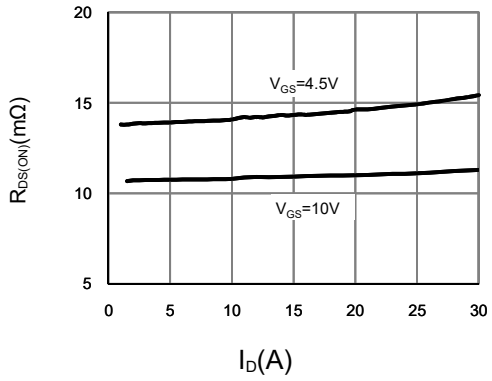


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

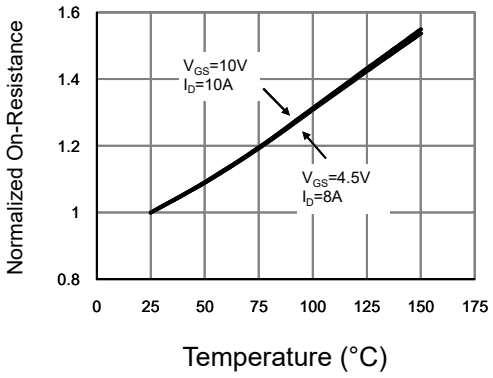


Figure 4: On-Resistance vs. Junction Temperature (Note E)

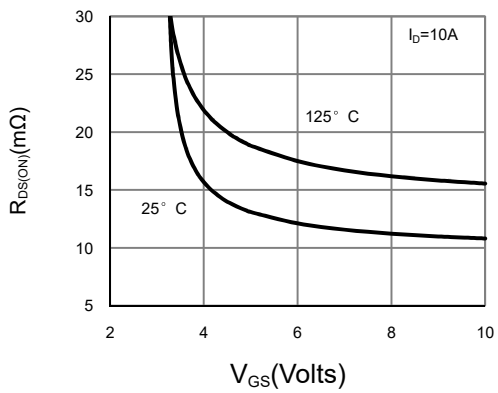


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

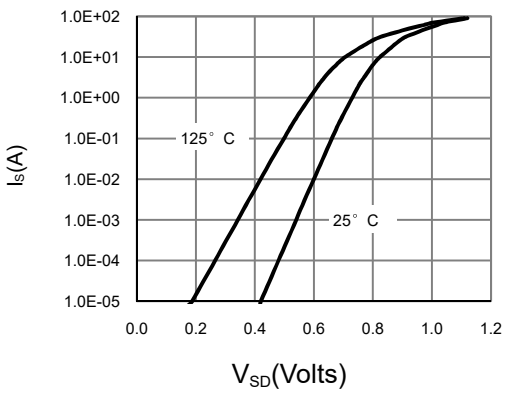


Figure 6: Body-Diode Characteristics (Note E)

7.2TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

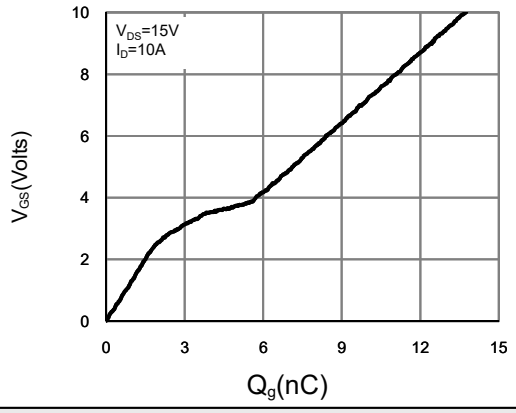


Figure 7: Gate-Charge Characteristics

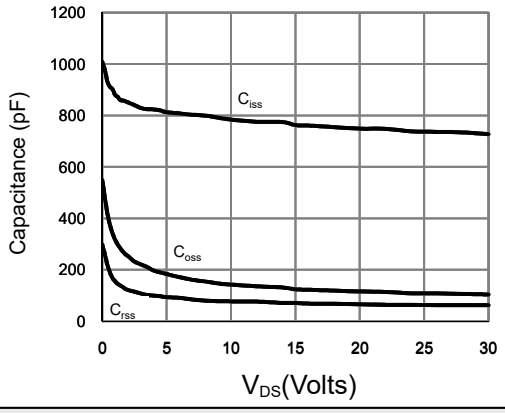


Figure 8: Capacitance Characteristics

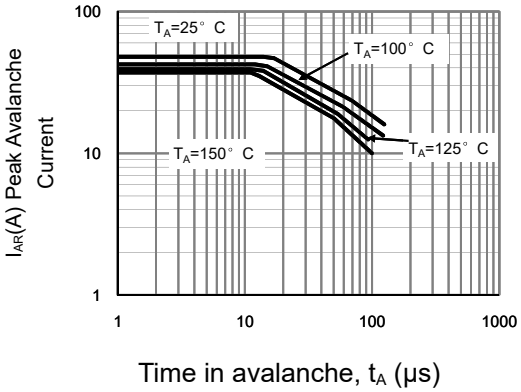


Figure 9: Single Pulse Avalanche capability (Note C)

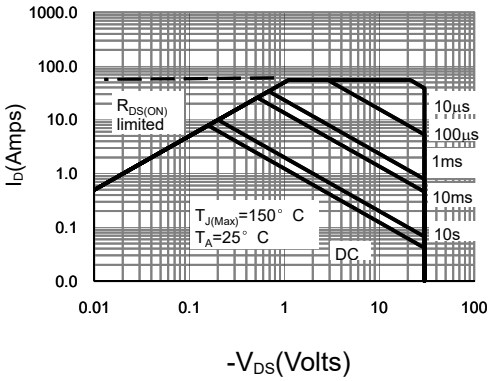


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

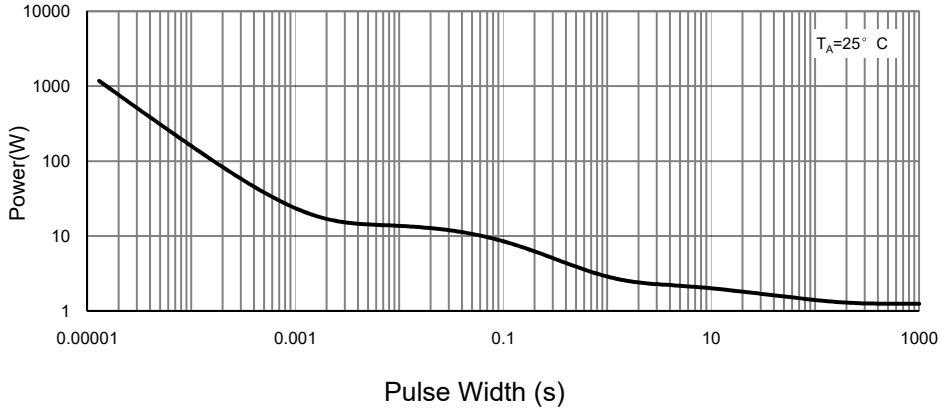


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

7.3TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

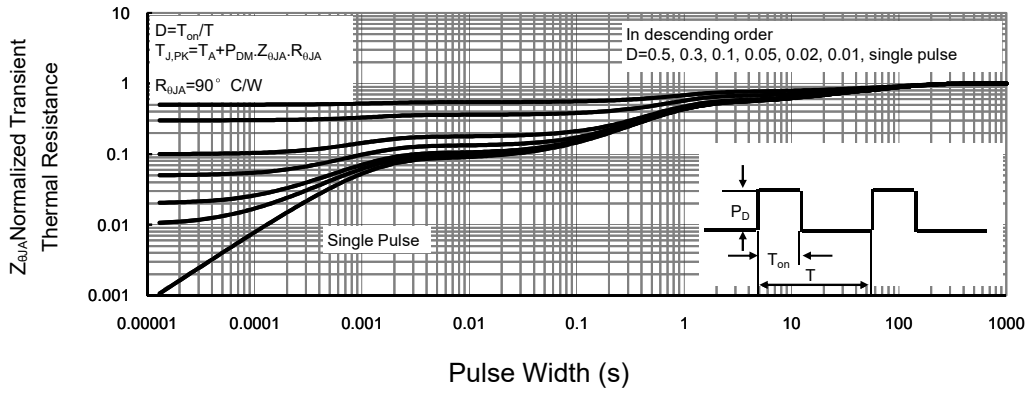
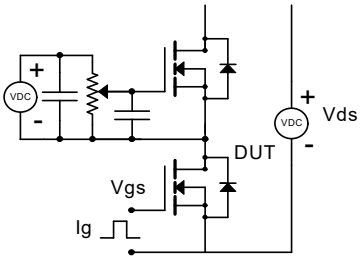
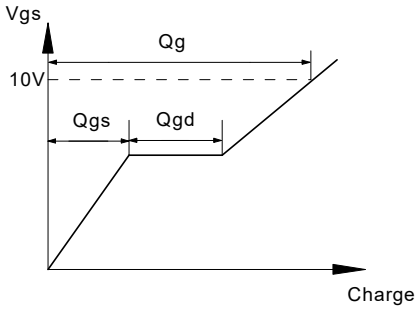


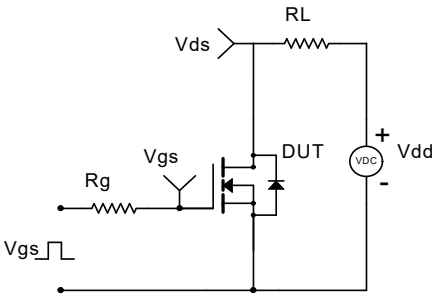
Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

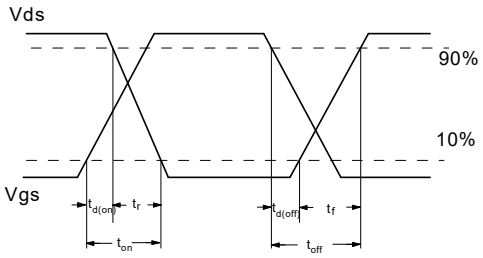
Gate Charge Test Circuit & Waveform



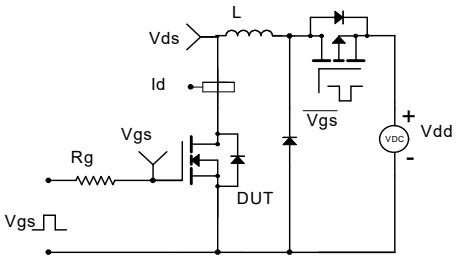


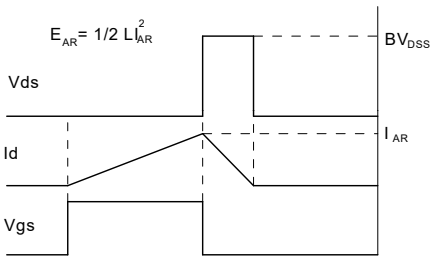
Resistive Switching Test Circuit & Waveforms



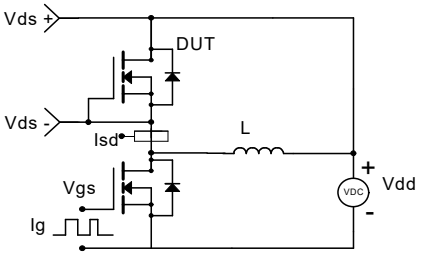


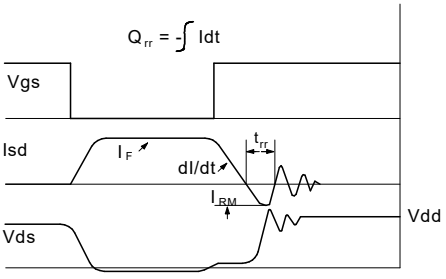
Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



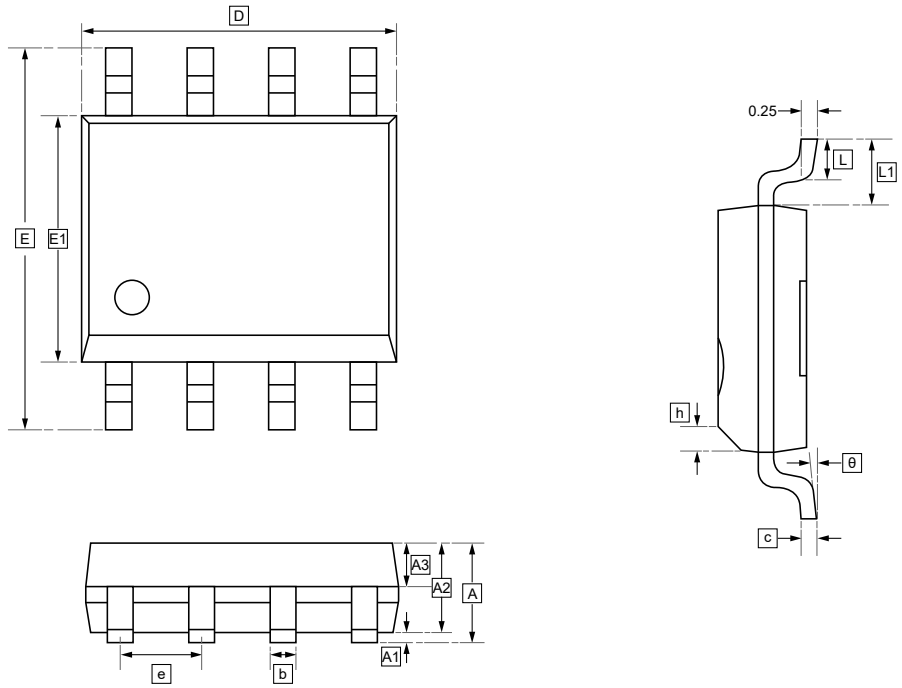


Diode Recovery Test Circuit & Waveforms





8.SOP-8 Package Outline Dimensions

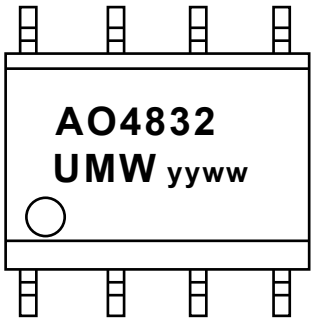


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.70	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.10	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW AO4832	SOP-8	3000	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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