UMW AO4606

30V N+P-Channel Enhancement Mode MOSFET

1.Description

The AO4606 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

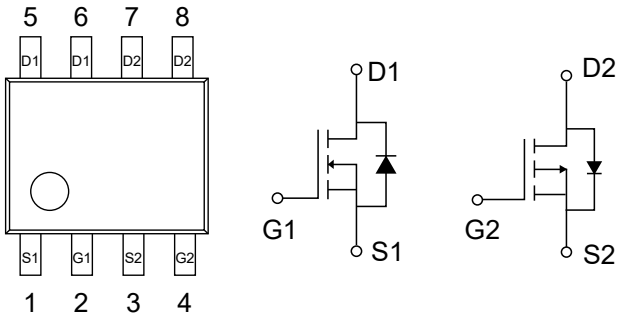
2.Features

- $V_{DS\ (V)}$=30V
- I_D=6A
- $R_{DS(ON)}$<28mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<42mΩ(V_{GS}=4.5V)
- $V_{DS\ (V)}$=-30V
- I_D=-7.6A
- $R_{DS(ON)}$<32mΩ(V_{GS}=10V)
- $R_{DS(ON)}$<40mΩ(V_{GS}=4.5V)

3.Pinning information

Pin	Symbol	Description
2,4	G1, G2	GATE
1,3	S1, S2	SOURCE
5,6,7,8	D1, D2	DRAIN

SOP-8



4.Absolute Maximum Ratings T_A= 25°C

Parameter		Symbol	Rating		Units
			N-Ch	P-Ch	
Drain-Source Voltage		V_{DS}	30	-30	V
Gate-Source Voltage		V_{GS}	±20	±20	V
Continuous Drain Current, V_{GS}=10V [1]	T_C=25°C	I_D	6	-7.6	A
Continuous Drain Current, V_{GS}=10V [1]	T_C=100°C		4.5	-5.9	A
Pulsed Drain Current [2]		I_{DM}	20	-15	A
Single Pulse Avalanche Energy [3]		E_{AS}	22	45	mJ
Avalanche Current		I_{AS}	21	-30	A
Total Power Dissipation [4]	T_C=25°C	P_D	2	2	W

Storage Temperature Range	T_{STG}	-55 to 150	-55 to 150	°C
Operating Junction Temperature Range	T_J	-55 to 150	-55 to 150	°C
Thermal Resistance Junction-Ambient [1]	$R_{\theta JA}$		62	°C/W
Thermal Resistance Junction-Case [1]	$R_{\theta JC}$		5	°C/W

5.1Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=250μA, V_{GS}=0V	30			V
BV_{DSS} Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25°C,I_D=1mA		0.023		V/°C
Static Drain-Source On-Resistance [2]	$R_{DS(ON)}$	V_{GS}=10V, I_D=6A		19	28	mΩ
		V_{GS}=4.5V, I_D=5A		28	42	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	1	1.7	2.5	V
$V_{GS(th)}$ Temperature Coefficient	$V_{GS(th)}$			-5.2		mV/°C
Drain-Source Leakage Current	I_{DSS}	V_{DS}=24V, V_{GS}=0V, T_J=25°C			1	μA
		V_{DS}=24V, V_{GS}=0V, T_J=55°C			5	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Forward Transconductance	g_{FS}	V_{DS}=5V, I_D=5A		16		S
Gate Resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz		2.5	5	Ω
Total Gate Charge (4.5V)	Q_g	V_{DS}=20V, V_{GS}=4.5V, I_D=5A		7.2		nC
Gate-Source Charge	Q_{gs}			1.4		nC
Gate-Drain Charge	Q_{gd}			2.2		nC
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=15V, V_{GS}=10V R_G=3.3Ω, I_D=5A		4.1		ns
Rise Time	t_r			9.8		ns
Turn-Off Delay Time	$t_{D(off)}$			15.5		ns
Fall Time	t_f			6		ns
Input Capacitance	C_{iss}	V_{DS}=15V, V_{GS}=0V, f=1MHz		572		pF
Output Capacitance	C_{oss}			81		pF
Reverse Transfer Capacitance	C_{rss}			65		pF
Continuous Source Current [1,5]	I_S	V_G=V_D=0V , Force Current			10	A
Pulsed Source Current [2,5]	I_{SM}				20	A
Diode Forward Voltage [2]	V_{SD}	V_{GS}=0V, I_S=1A, T_J=25°C			1.2	V

1.The data tested by surface mounted on a 1 inch [2] FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%

3.The EAS data shows Max. rating . The test condition is V_{DD}=25V,V_{GS}=10V,L=0.1mH,I_{AS}=21A

4 .The power dissipation is limited by 150°C junction temperature

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

5.2Electrical Characteristic (T_J=25°C unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Drain-Source Breakdown Voltage	BV_{DSS}	I_D=-250μA, V_{GS}=0V	-30			V
BV_{DSS} Temperature Coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference to 25°C,I_D=1mA		-0.021		V/°C
Static Drain-Source On-Resistance [2]	$R_{DS(ON)}$	V_{GS}=-10V, I_D=-7A		24	32	mΩ
		V_{GS}=-4.5V, I_D=-5A		32	40	mΩ
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-1	-1.6	-2.5	V
$V_{GS(th)}$ Temperature Coefficient	$V_{GS(th)}$			-4.2		mV/°C
Drain-Source Leakage Current	I_{DSS}	V_{DS}=-24V, V_{GS}=0V, T_J=25°C			-1	μA
		V_{DS}=-24V, V_{GS}=0V, T_J=55°C			-5	μA
Gate-Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Forward Transconductance	g_{FS}	V_{DS}=-5V, I_D=-7A		15		S
Gate Resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz		15	30	Ω
Total Gate Charge (-4.5V)	Q_g	V_{DS}=-20V		9.8		nC
Gate-Source Charge	Q_{gs}	V_{GS}=-4.5V		2.2		nC
Gate-Drain Charge	Q_{gd}	I_D=-7A		3.4		nC
Turn-On Delay Time	$t_{D(on)}$	V_{DD}=-15V, V_{GS}=-10V		16.4		ns
Rise Time	t_r			20.2		ns
Turn-Off Delay Time	$t_{D(off)}$	R_G=3.3Ω, I_D=-5A		55		ns
Fall Time	t_f			10		ns
Input Capacitance	C_{iss}	V_{DS}=-15V, V_{GS}=0V, f=1MHz		930		pF
Output Capacitance	C_{oss}			148		pF
Reverse Transfer Capacitance	C_{rss}			115		pF
Continuous Source Current [1,5]	I_S	V_G=V_D=0V , Force Current			-7.6	A
Pulsed Source Current [2,5]	I_{SM}				-15	A
Diode Forward Voltage [2]	V_{SD}	V_{GS}=0V, I_S=-1A, T_J=25°C			-1.2	V

1.The data tested by surface mounted on a 1 inch [2] FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width ≤ 300us , duty cycle ≤ 2%.

3.The EAS data shows. The power dissipation is limited by ows Max. rating.

4. The test condition is V150°C junction temperature V_{DD}=-25 V,V_{GS}=-10V,L=0.1mH,I_{AS}=-30A.

5 .The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

7.1Typical characteristic

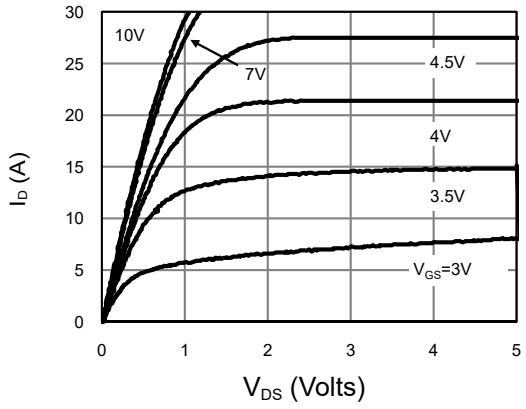


Fig.1 On-Region Characteristics

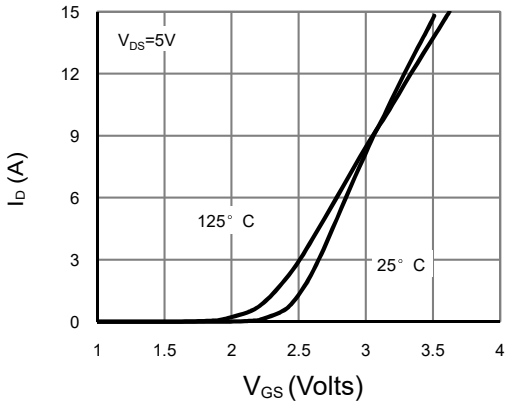


Fig.2 Transfer Characteristics

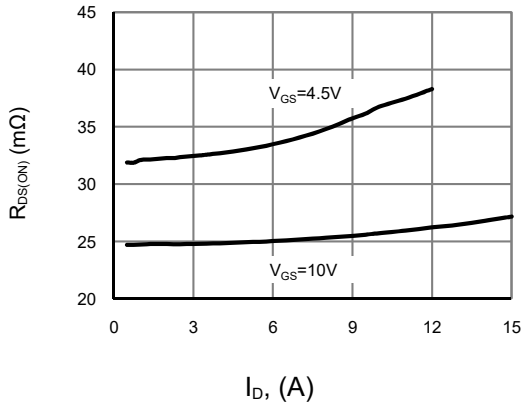


Fig.3 On-Resistance vs. Drain Current and Gate Voltage

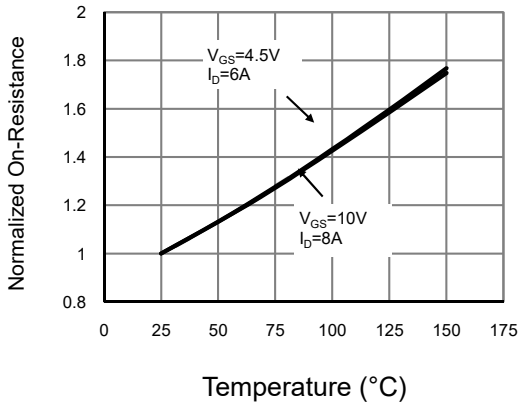


Fig.4 On-Resistance vs. Junction Temperature

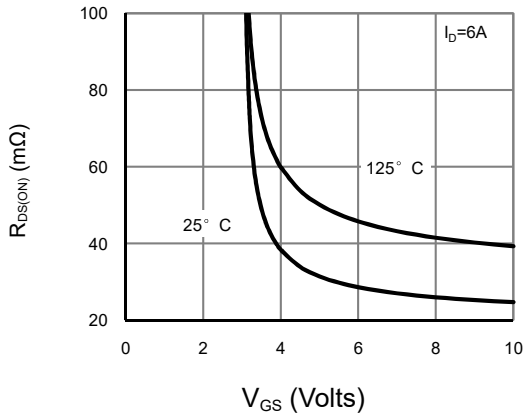


Fig.5 On-Resistance vs. Gate-Source Voltage

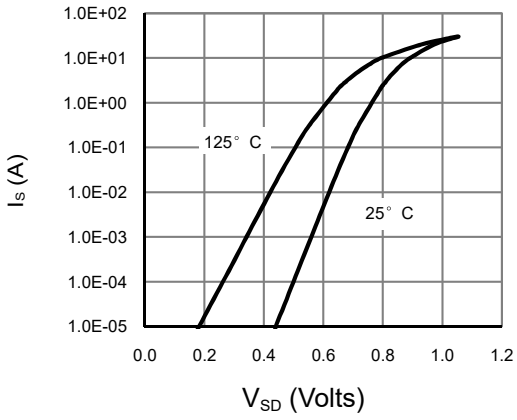


Fig.6 Body-Diode Characteristics

7.2Typical characteristic

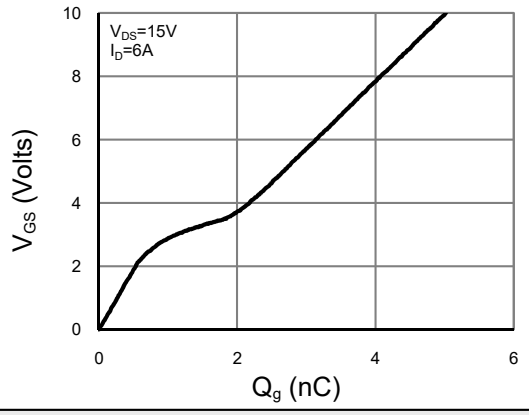


Fig.7 Gate-Charge Characteristics

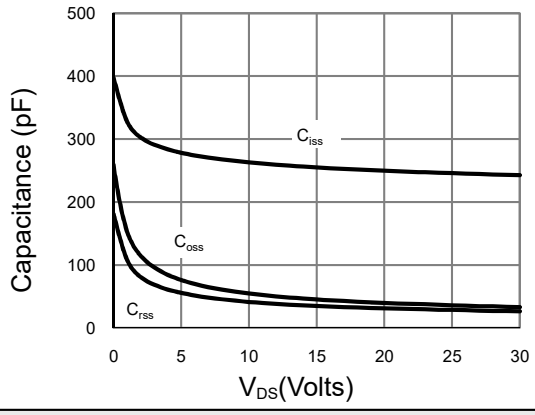


Fig.8 Capacitance Characteristics

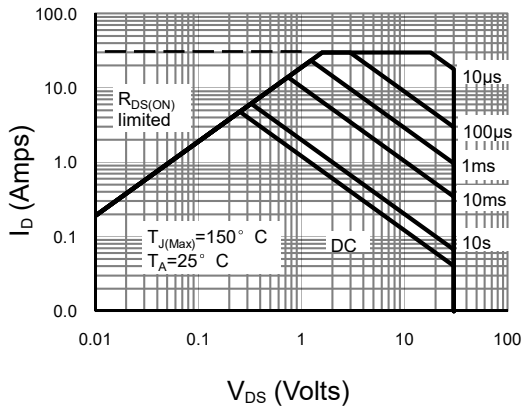


Fig.9 Maximum Forward Biased Safe Operating Area

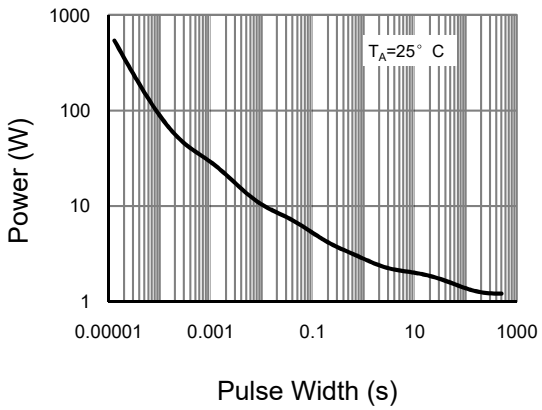


Fig.10 Single Pulse Power Rating Junction-to-Ambient

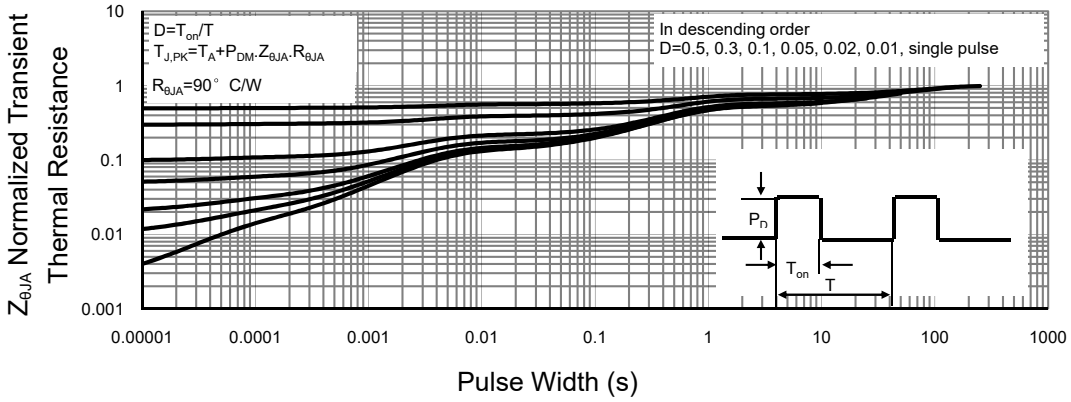


Fig.11 Normalized Maximum Transient Thermal Impedance

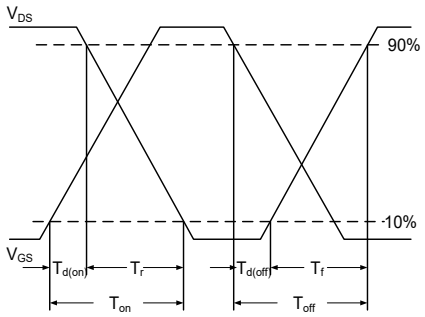


Fig.12 Switching Time Waveform

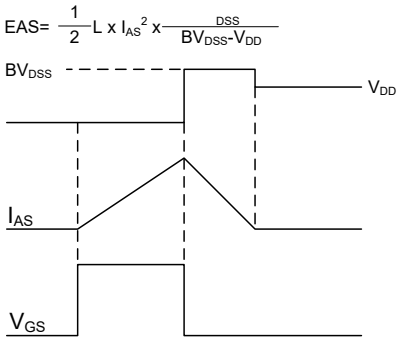


Fig.13 Unclamped Inductive Switching Waveform

7.3Typical characteristic

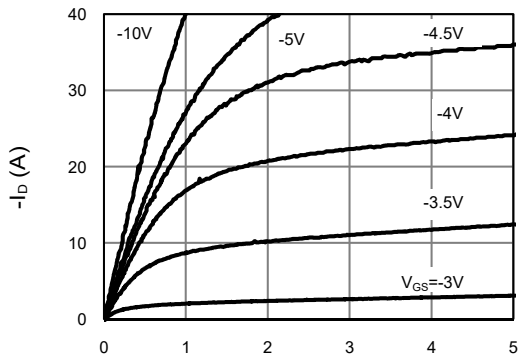


Fig.14 On-Region Characteristics

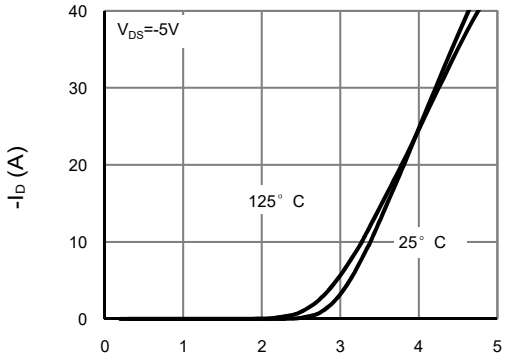


Fig. 15 Transfer Characteristics

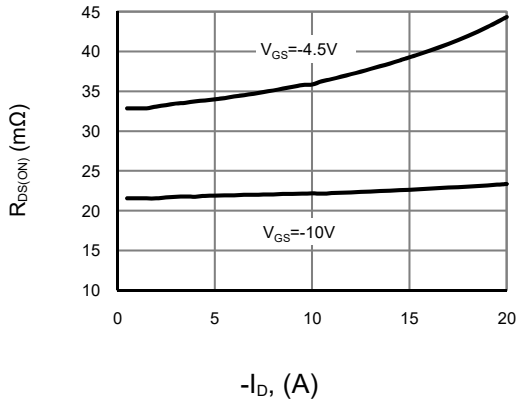


Fig.16 On-Resistance vs. Drain Current and Gate Voltage

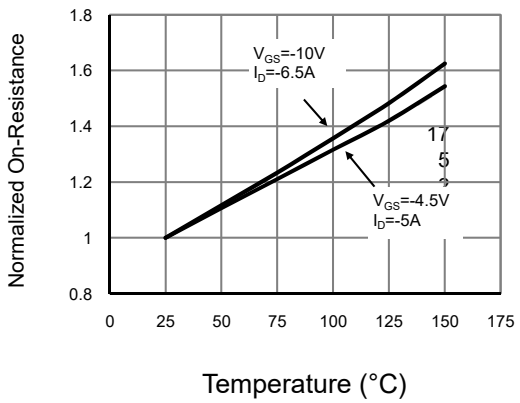


Fig.17 On-Resistance vs. Junction Temperature

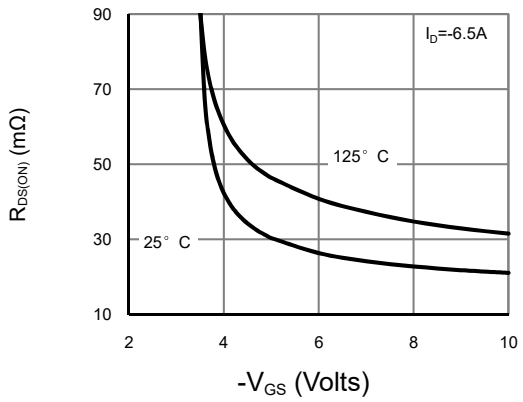


Fig.18 On-Resistance vs. Gate-Source Voltage

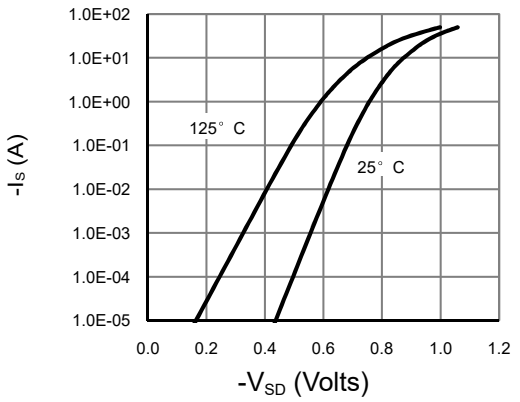


Fig.19 Body-Diode Characteristics

7.4Typical characteristic

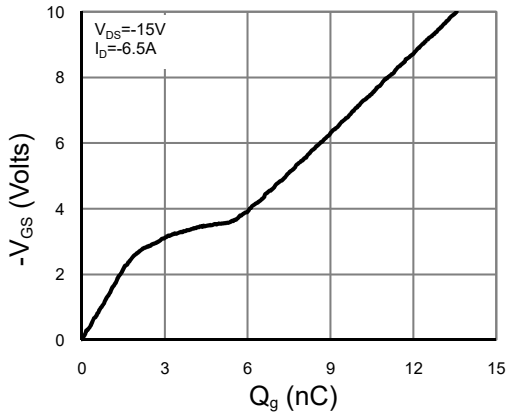


Fig.20 Gate-Charge Characteristics

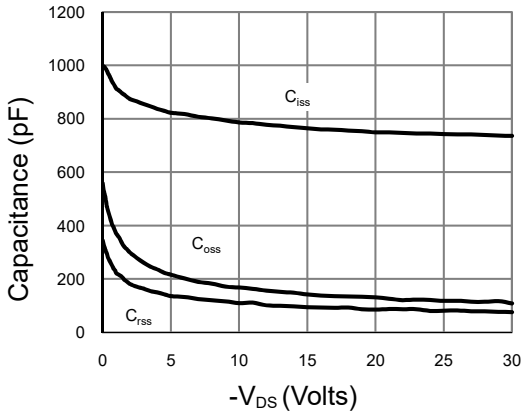


Fig.21 Capacitance Characteristics

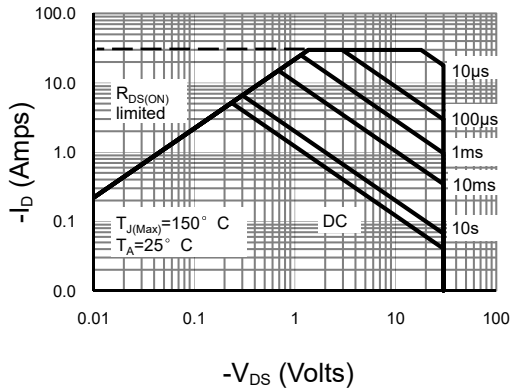


Fig.22 Maximum Forward Biased Safe Operating Area

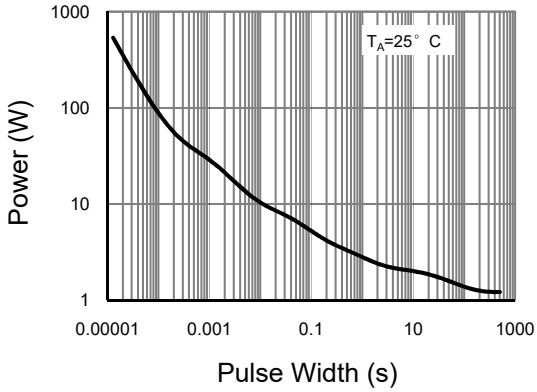


Fig.23 Single Pulse Power Rating Junction-to-Ambient

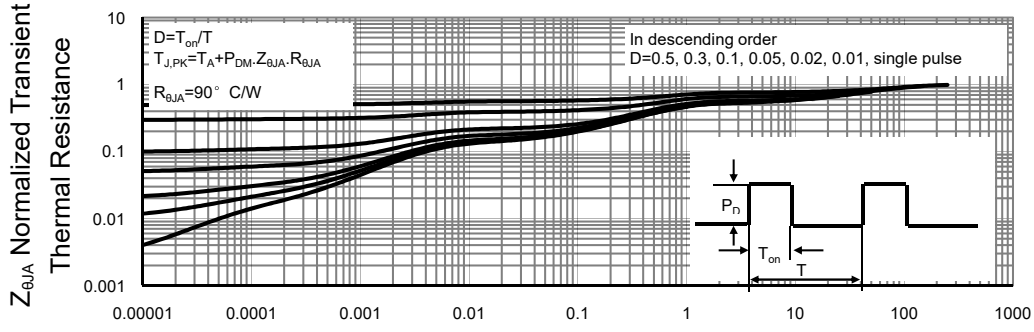


Fig.24 Normalized Maximum Transient Thermal Impedance

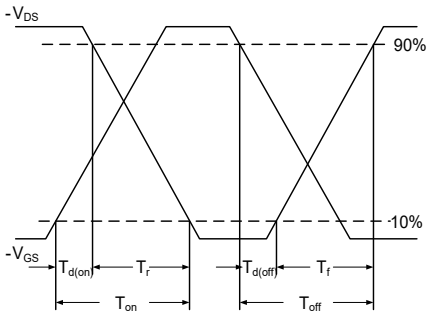


Fig.25 Switching Time Waveform

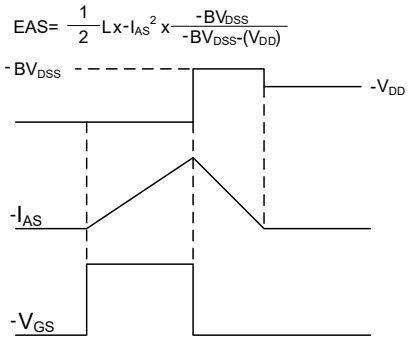
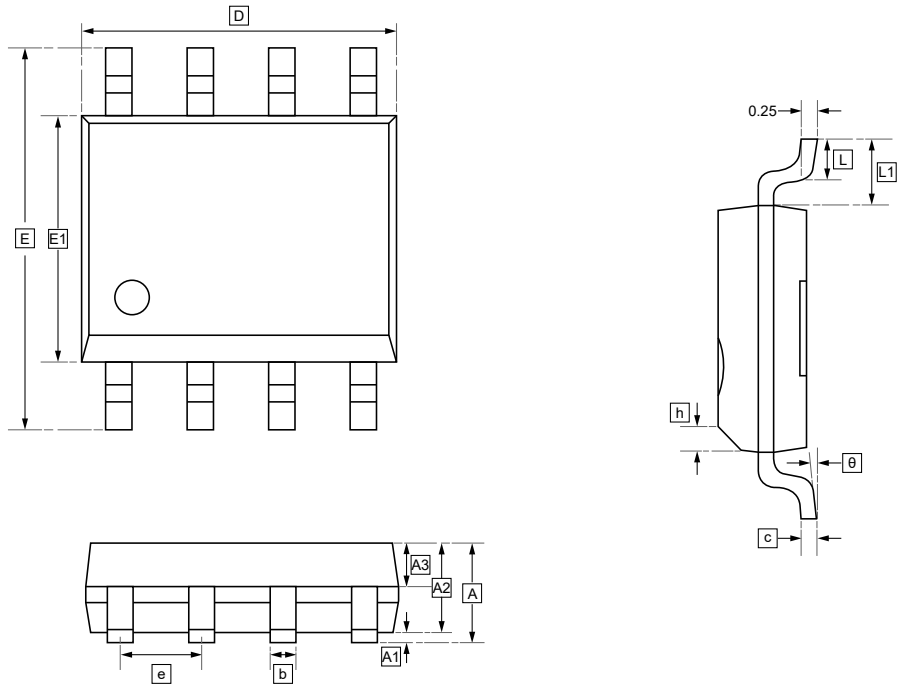


Fig.26 Unclamped Inductive Switching Waveform

8.SOP-8 Package Outline Dimensions

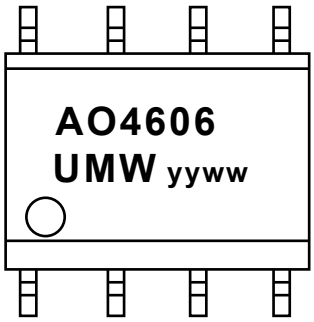


DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	A3	b	c	D	E	E1	e	h	L
Min	-	0.05	1.30	0.60	0.39	0.20	4.70	5.80	3.80	1.24	0.30	0.50
Max	1.75	0.20	1.50	0.70	0.47	0.24	5.10	6.20	4.00	1.30	0.50	0.80

Symbol	L1	θ
Min	1.00	0°
Max	1.10	8°

9.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW AO4606	SOP-8	3000	Tape and reel

10.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

When applying our products, please do not exceed the maximum rated values, as this may affect the reliability of the entire system. Under certain conditions, any semiconductor product may experience faults or failures. Buyers are responsible for adhering to safety standards and implementing safety measures during system design, prototyping, and manufacturing when using our products to prevent potential failure risks that could lead to personal injury or property damage.

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