1.Description

This single analog switch is designed for 1.65-V to 5.5-V V_{CC} operation. The SN74LVC1G66 device can handle analog and digital signals. The device permits bidirectional transmission of signals with amplitudes of up to 5.5V(peak). NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

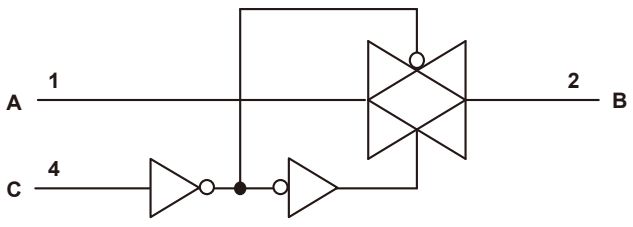
2.Applications

- Wireless Devices
- Audio and Video Signal Routing
- Portable Computing
- Wearable Devices
- Signal Gating, Chopping, Modulation or Demodulation (Modem)
- Signal Multiplexing for Analog-to-Digital and Digital-to-Analog Conversion Systems

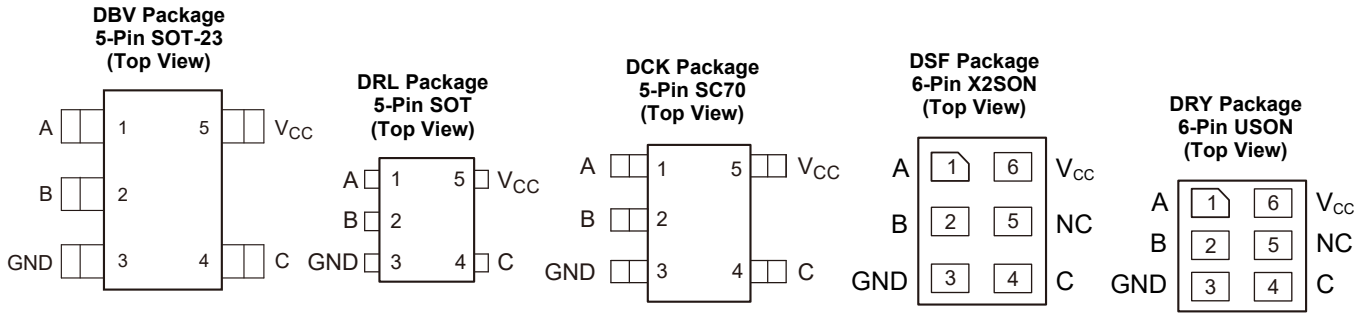
3.Features

- 1.65-V to 5.5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max tpd of 0.8 ns at 3.3 V
- High On-Off Output Voltage Ratio
- High Speed, Typically 0.5ns (V_{CC}=3V, C_L=50pF)
- Low ON-State Resistance, Typically≈5.5Ω (V_{CC}=4.5V)
- High Degree of Linearity
- Latch-Up Performance Exceeds 100mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  – 2000-V Human-Body Model (A114-A)
  – 200-V Machine Model (A115-A)
  – 1000-V Charged-Device Model (C101)

4.Logic Diagram (Positive Logic)



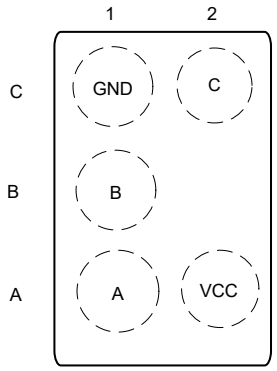
5.1 Pinning Information



Pin Functions

Pin			I/O	Description
Name	SOT NO.	USON, X2SON NO.		
A	1	1	I/O	Bidirectional signal to be switched
B	2	2	I/O	Bidirectional signal to be switched
C	4	4	I	Controls the switch (L=OFF, H=ON)
GND	3	3	-	Ground pin
NC	-	5	-	Do not connect
V_{CC}	5	6	-	Power pin

5.2 Pinning Information



YZP Package
5-Pin DSBGA (Bottom View)

Pin Functions

Pin		I/O	Description
Name	DSBGA NO.		
A	A1	I/O	Bidirectional signal to be switched
B	B1	I/O	Bidirectional signal to be switched
C	C2	I	Controls the switch (L=OFF, H=ON)
GND	C1	-	Ground pin
V_{CC}	A2	-	Power pin

6.Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Symbol	Min	Max	Units
Supply voltage (2)		V_{CC}	-0.5	6.5	V
Input voltage (2)(3)		V_I	-0.5	6.5	V
Switch I/O voltage (2)(3)(4)		$V_{I/O}$	-0.5	V_{CC}+0.5	V
Control input clamp current	V_I<0	I_{IK}		-50	mA
I/O port diode current	$V_{I/O}$<0 or $V_{I/O}$>V_{CC}	I_{IOK}		±50	mA
ON-state switch current	$V_{I/O}$<0 to V_{CC}	I_T		±50	mA
Continuous current through V_{CC} or GND				±100	mA
Storage Temperature		T_{STG}	-65	150	°C
Junction Temperature		T_J		150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to ground, unless otherwise specified.

(3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(4) This value is limited to 5.5 V maximum.

7.ESD Ratings

Parameter		Symbol	Value	Units
Electrostatic Discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	$V_{(ESD)}$	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)		±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted) (1)

Condition		Symbol	Min	Max	Unit
Supply voltage		V_{CC}	1.65	5.5	V
I/O port voltage		$V_{I/O}$	0	V_{CC}	V
High-level input voltage, control input	V_{CC}=1.65V to 1.95V	V_{IH}	V_{CC}×0.65		V
	V_{CC}=2.3V to 2.7V		V_{CC}×0.7		V
	V_{CC}=3V to 3.6V		V_{CC}×0.7		V
	V_{CC}=4.5V to 5.5V		V_{CC}×0.7		V
Low-level input voltage, control input	V_{CC}=1.65V to 1.95V	V_{IL}		V_{CC}x0.35	V
	V_{CC}=2.3V to 2.7V			V_{CC}x0.3	V
	V_{CC}=3V to 3.6V			V_{CC}x0.3	V
	V_{CC}=4.5V to 5.5V			V_{CC}x0.3	V
Control input voltage		V_I	0	5.5	V
Control input transition rise and fall time	V_{CC}=1.65V to 1.95V	Δt/Δv		20	ns/V
	V_{CC}=2.3V to 2.7V			20	ns/V
	V_{CC}=3V to 3.6V			10	ns/V
	V_{CC}=4.5V to 5.5V			10	ns/V
Operating free-air temperature		T_A	-40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

9.ESD Ratings

Parameter	DBV (SOT-23)	DCK (SC70)	DRL (SOT)	DRY (USON)	DSF (X2SON)	YZP (DSBGA)	Units
	5 PINS	5 PINS	5 PINS	6 PINS	6 PINS	5 PINS	
Junction-to-ambient thermal resistance, $R_{\theta JA}$	206	252	142	-	-	132	°C/W

10.Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

Parameter	Symbol	Conditions		V_{CC}	Min	Typ(1)	Max	Units
ON-state switch resistance	r_{on}	V_I=V_{CC} or GND, V_C=V_{IH} (see Figure 2 and Figure 1)	I_S=4mA	1.65V		12	30	Ω
			I_S=8mA	2.3V		9	20	Ω
			I_S=24mA	3V		7.5	15	Ω
			I_S=32mA	4.5V		5.5	10	Ω
Peak on resistance	$r_{on(p)}$	V_I=V_{CC} or GND, V_C=V_{IH} (see Figure 2 and Figure 1)	I_S=4mA	1.65V		74.5	120	Ω
			I_S=8mA	2.3V		20	30	Ω
			I_S=24mA	3V		11.5	20	Ω
			I_S=32mA	4.5V		7.5	15	Ω
OFF-state switch leakage current	$I_{S(off)}$	V_I=V_{CC} and V_O=GND or V_I= GND and V_O=V_{CC} V_C=V_{IL} (see Figure 3)		5.5V			±1	μA
			T_A=25°C				±0.1	μA
ON-state switch leakage current	$I_{S(on)}$	V_I=V_{CC} or GND, V_C=V_{IH}, V_O=Open (see Figure 4)		5.5V			±1	μA
			T_A=25°C				±0.1	μA
Control input current	I_I	V_C=V_{CC} or GND		5.5V			±1	μA
			T_A=25°C				±0.1	μA
Supply current	I_{CC}	V_C=V_{CC} or GND		5.5V			10	μA
			T_A=25°C				1	μA
Supply current change	ΔI_{CC}	V_C=V_{CC} – 0.6V		5.5V			500	μA
Control input capacitance	C_{iC}			5V		2		pF
Switch input and output capacitance	$C_{io(off)}$			5V		6		pF
Switch input and output capacitance	$C_{io(on)}$			5V		13		pF

(1) T_A=25°C

11.Switching Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

Parameter	From (Input)	To (Output)	V_{CC}=1.8V±0.15V		V_{CC}=2.5V±0.2V		V_{CC}=3.3V±0.3V		V_{CC}=5V±0.5V		Units
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{pd} (1)	A or B	B or A		2		1.2		0.8		0.6	ns
t_{pd} (2)	C	A or B	2.5	12	1.9	6.5	1.8	5	1.5	4.2	ns
t_{pd} (3)	C	A or B	2.2	10	1.4	6.9	2	6.5	1.4	5	ns

(1) t_{PLH} and t_{PHL} are the same as t_{pd}. The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

(2) t_{PZL} and t_{PZH} are the same as t_{en}.

(3) t_{PLZ} and t_{PHZ} are the same as t_{dis}.

12.Analog Switch Characteristics (T_A=25°C)

Parameter	From (Input)	To (Output)	Conditions	V_{CC}	Typ	Units
Frequency response (1) (switch ON)	A or B	B or A	C_L=50pF, R_L=600Ω, f_{in}=sine wave	1.65V	35	MHz
				2.3V	120	MHz
				3V	175	MHz
				4.5V	195	MHz
			C_L=5pF, R_L=50Ω, f_{in}=sine wave	1.65V	>300	MHz
				2.3V	>300	MHz
				3V	>300	MHz
				4.5V	>300	MHz
Crosstalk (control input to signal output)	C	A or B	C_L=50pF, R_L=600Ω, f_{in}=1MHz (square wave)	1.65V	35	mV
				2.3V	50	mV
				3V	70	mV
				4.5V	100	mV
Feedthrough attenuation (2) (switch OFF)	A or B	B or A	C_L=50pF, R_L=600Ω, f_{in}=1MHz (sine wave)	1.65V	-58	dB
				2.3V	-58	dB
				3V	-58	dB
				4.5V	-58	dB
			C_L=5pF, R_L=50Ω, f_{in}=1MHz (sine wave)	1.65V	-42	dB
				2.3V	-42	dB
				3V	-42	dB
				4.5V	-42	dB

Parameter	From (Input)	To (Output)	Conditions	V_{CC}	Typ	Units
Sine-wave distortion	A or B	B or A	C_L=50pF, R_L=10kΩ, f_{in}=1kHz (sine wave)	1.65V	0.1%	
				2.3V	0.025%	
				3V	0.015%	
				4.5V	0.01%	
			C_L=50pF, R_L=10kΩ, f_{in}=10kHz (sine wave)	1.65V	0.15%	
				2.3V	0.025%	
				3V	0.015%	
				4.5V	0.01%	

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads –3 dB.

(2) Adjust f_{in} voltage to obtain 0 dBm at input.

13.Operating Characteristics (T_A=25°C)

Parameter	Test Conditions	V_{CC}=1.8V	V_{CC}=2.5V	V_{CC}=3.3V	V_{CC}=5V	Units
		Typ	Typ	Typ	Typ	
Power dissipation capacitance, C_{pd}	f=10MHz	8	9	9	11	pF

14.Typical Characteristics (T_A=25°C)

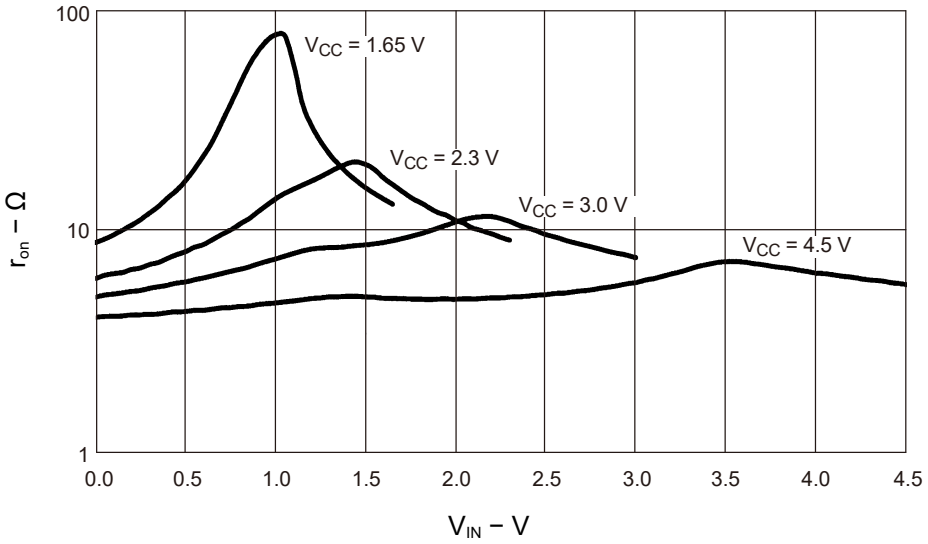


Figure 1. Typical r_{on} as a Function of Input Voltage (V_I) for V_I=0 to V_{CC}

15.Parameter Measurement Information

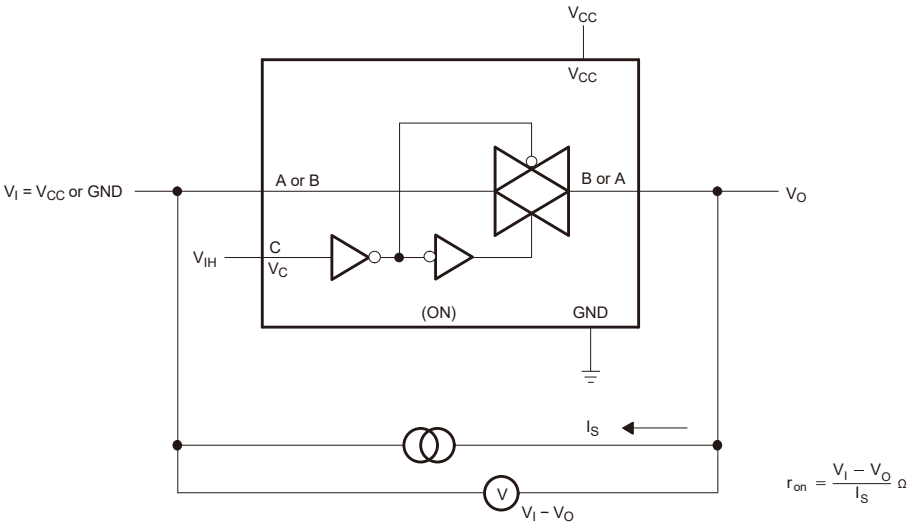


Figure 2. ON-State Resistance Test Circuit

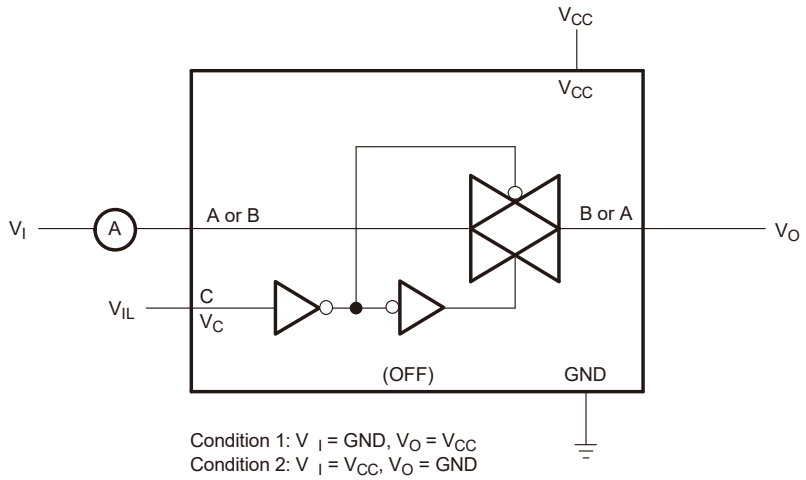


Figure 3. OFF-State Switch Leakage-Current Test Circuit

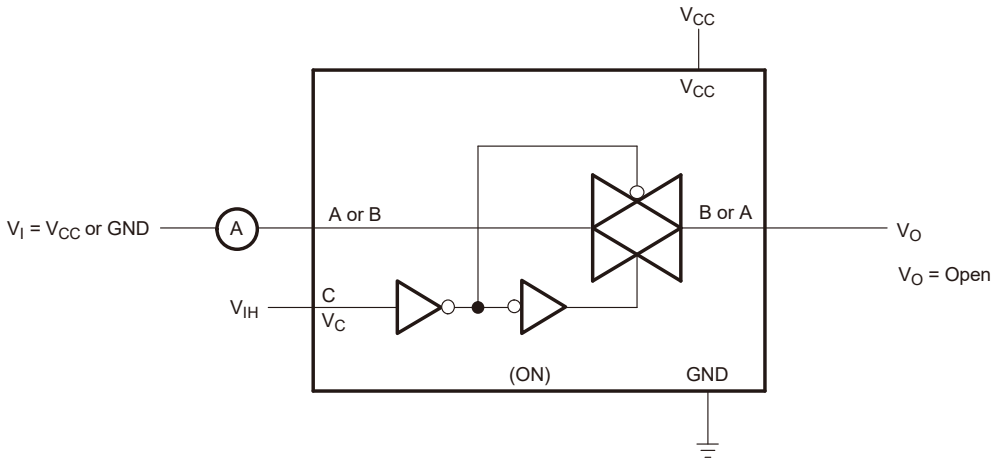
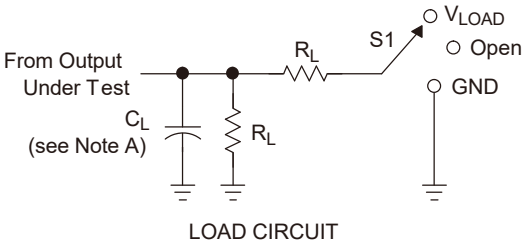


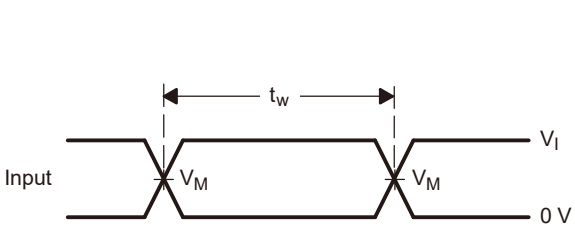
Figure 4. ON-State Switch Leakage-Current Test Circuit



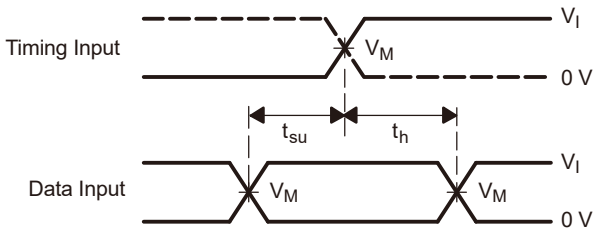
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

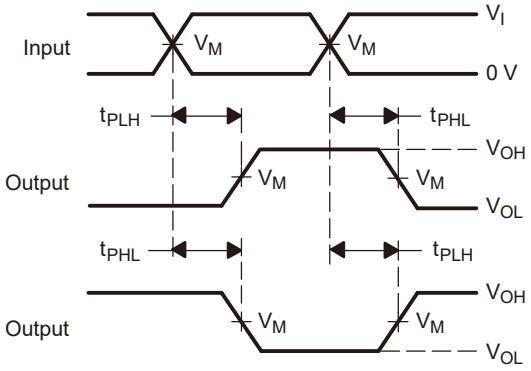
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V
	V_I	t_r/t_f					
1.8 V 0.15 V	V_{CC}	2 ns	$V_{CC}/2$	2 V_{CC}	30 pF	1 k	0.15 V
2.5 V 0.2 V	V_{CC}	2 ns	$V_{CC}/2$	2 V_{CC}	30 pF	500	0.15 V
3.3 V 0.3 V	V_{CC}	2.5 ns	$V_{CC}/2$	2 V_{CC}	50 pF	500	0.3 V
5 V 0.5 V	V_{CC}	2.5 ns	$V_{CC}/2$	2 V_{CC}	50 pF	500	0.3 V



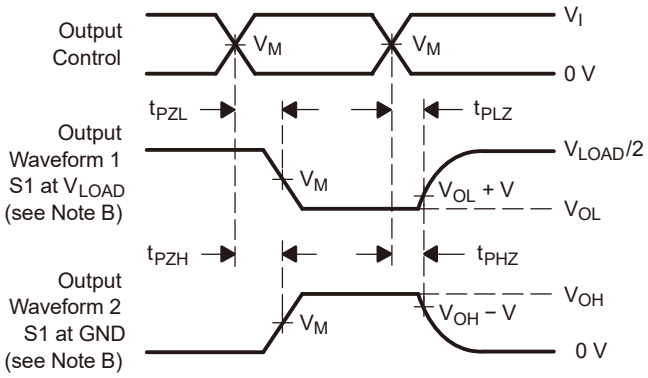
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:

A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.

F. t_{PZL} and t_{PZH} are the same as t_{en}.

G. t_{PLH} and t_{PHL} are the same as t_{pd}.

H. All parameters and waveforms are not applicable to all devices

Figure 5. Load Circuit and Voltage Waveforms

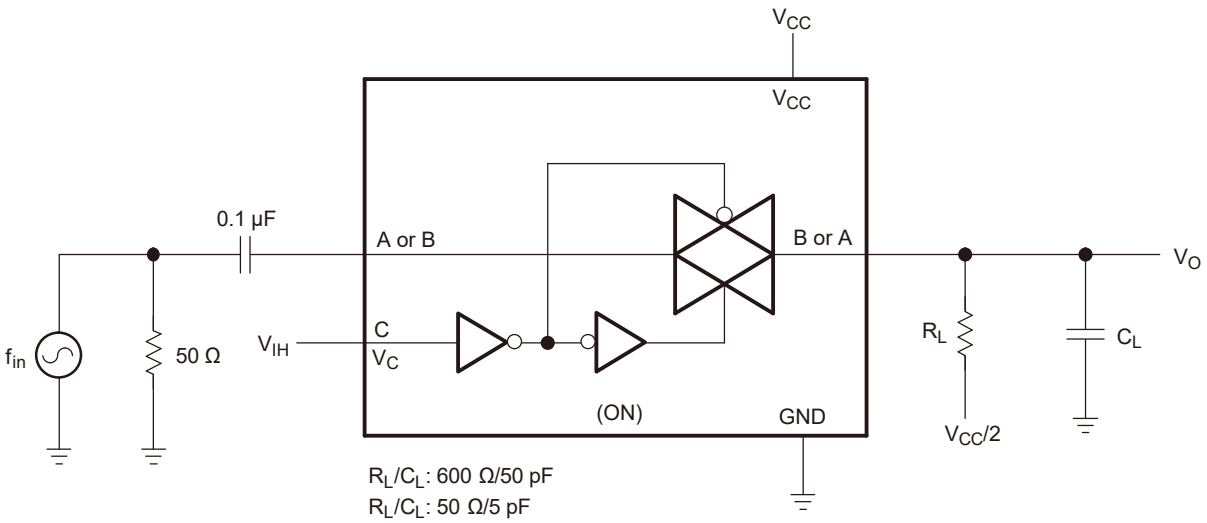


Figure 6. Frequency Response (Switch ON)

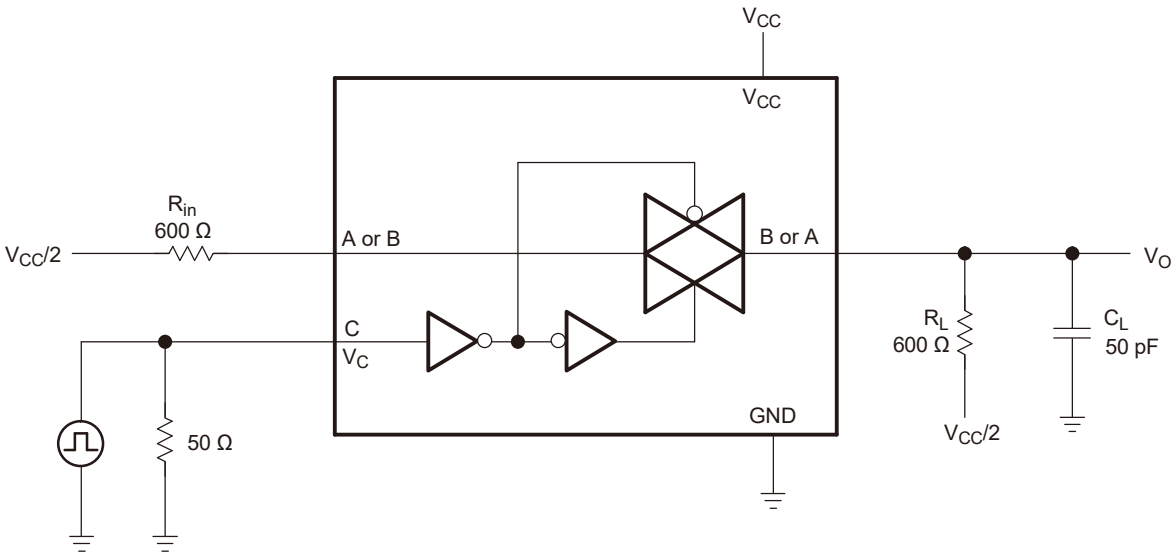


Figure 7. Crosstalk (Control Input – Switch Output)

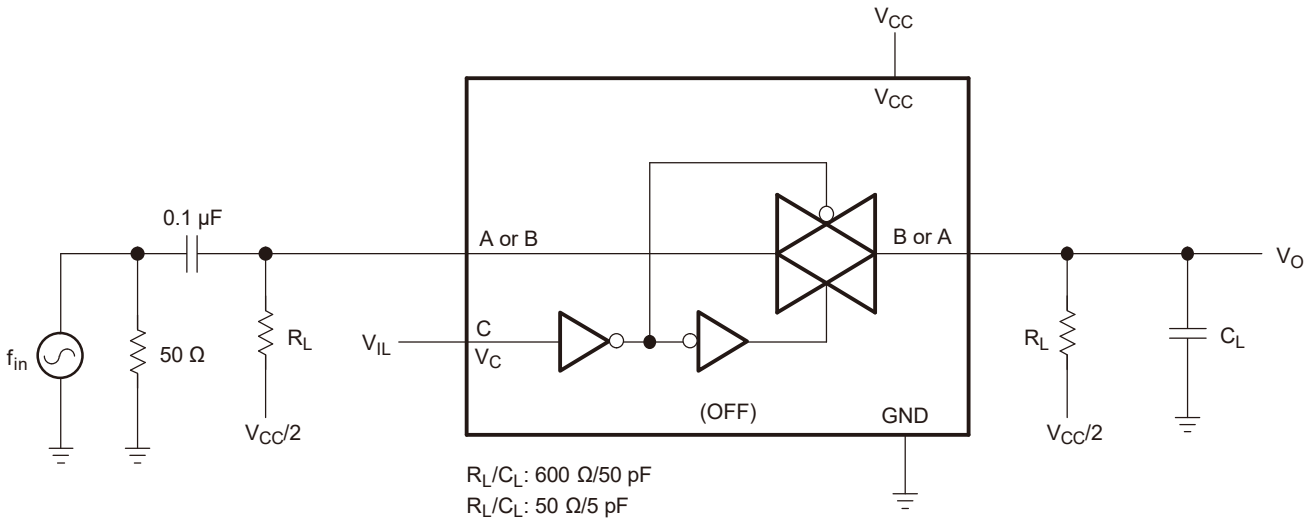


Figure 8. Feedthrough (Switch OFF)

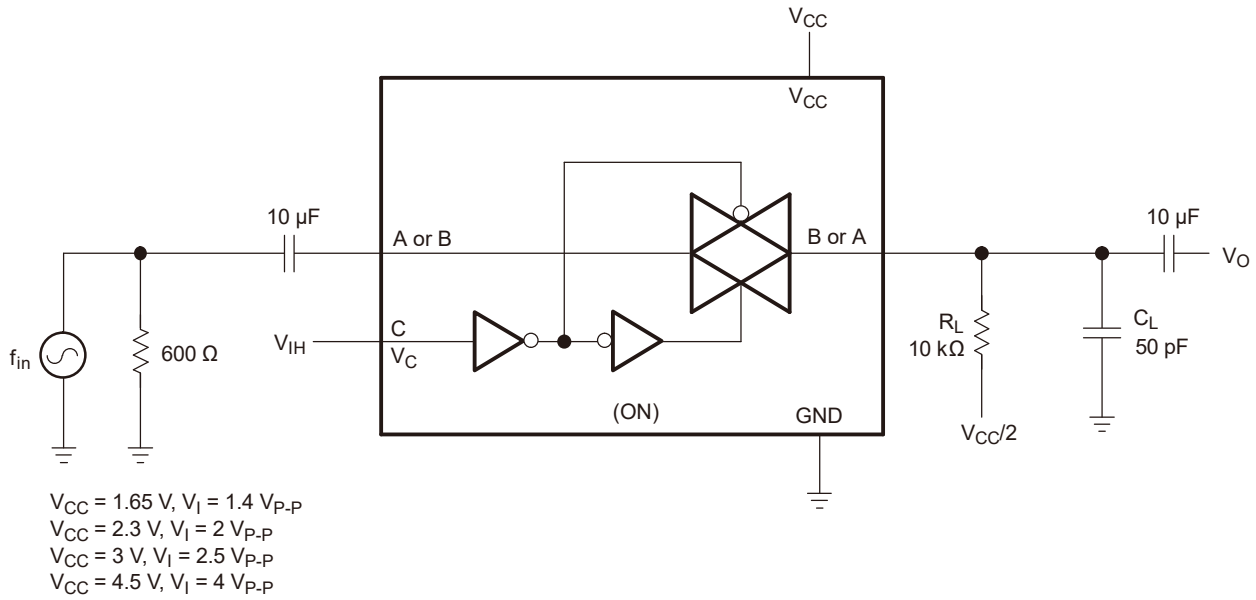


Figure 9. Sine-Wave Distortion

16.Detailed Description

Overview

This single analog switch is designed for 1.65-V to 5.5-V V_{CC} operation.

The SN74LVC1G66 device can handle analog and digital signals. The device permits bidirectional transmission of signals with amplitudes of up to 5.5V (peak). Like all analog switches, the SN74LVC1G66 is bidirectional.

Functional Block Diagram

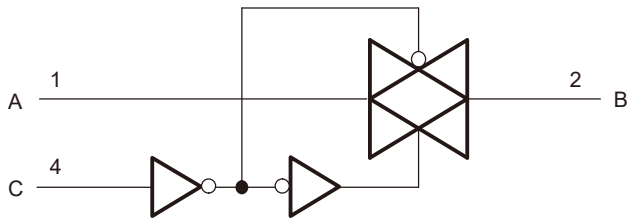


Figure 10. Logic Diagram (Positive Logic)

Feature Description

The SN74LVC1G66 has a wide V_{CC} range, allowing rail-to-rail operation of signals anywhere from a 1.8-V system to a 5-V system. In addition, the control input (C Pin) is 5.5-V tolerant, allowing higher-voltage logic to interface to the switch control system.

Device Functional Modes

Table 1. Function Table

CONTROL INPUT (C)	SWITCH
L	OFF
H	ON

Application Information

The SN74LVC1G66 can be used in any situation where an SPST switch would be used and a solid-state, voltage-controlled version is preferred

Typical Application

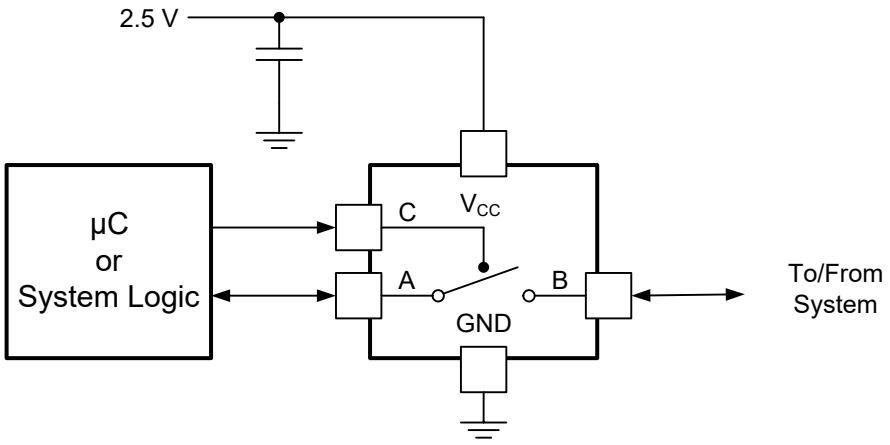


Figure 11. Typical Application Schematic

Design Requirements

The SN74LVC1G66 allows on and off control of analog and digital signals with a digital control signal. All input signals should remain between 0 V and V_{CC} for optimal operation.

Application Curve

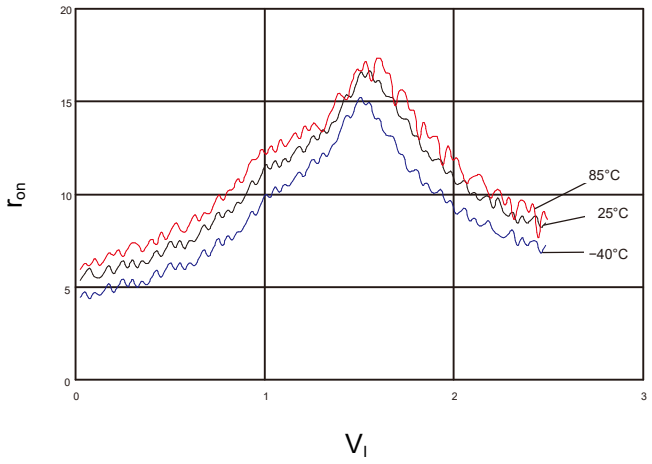
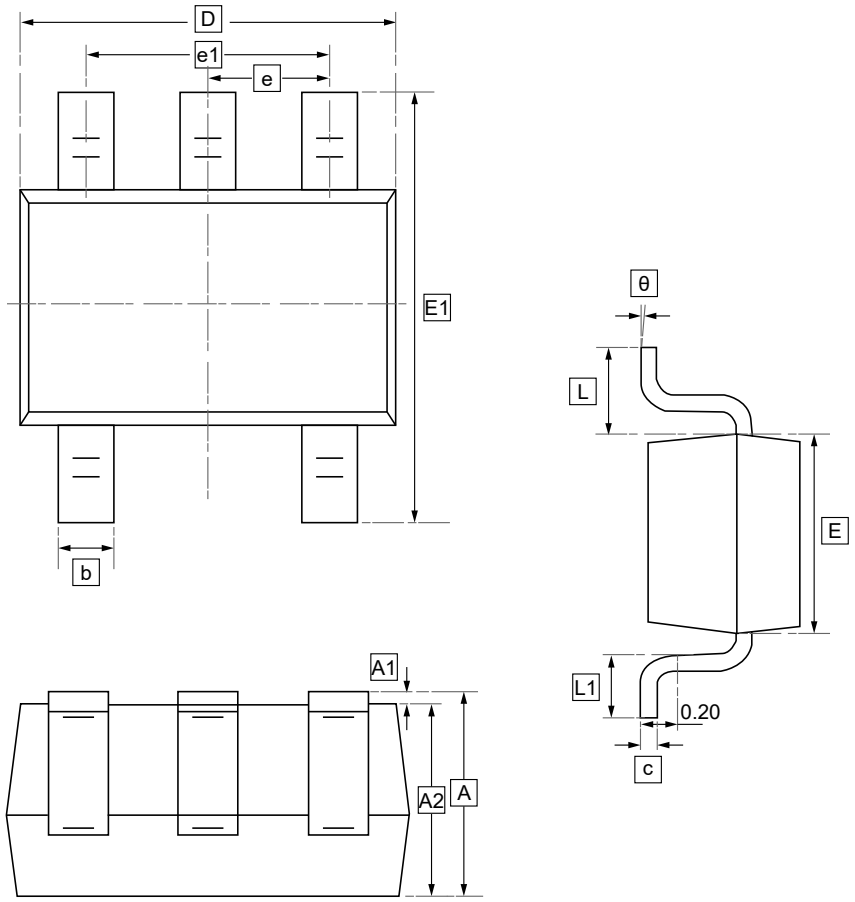


Figure 12. r_{on} vs V_I, V_{CC}=2.5V (SN74LVC1G66)

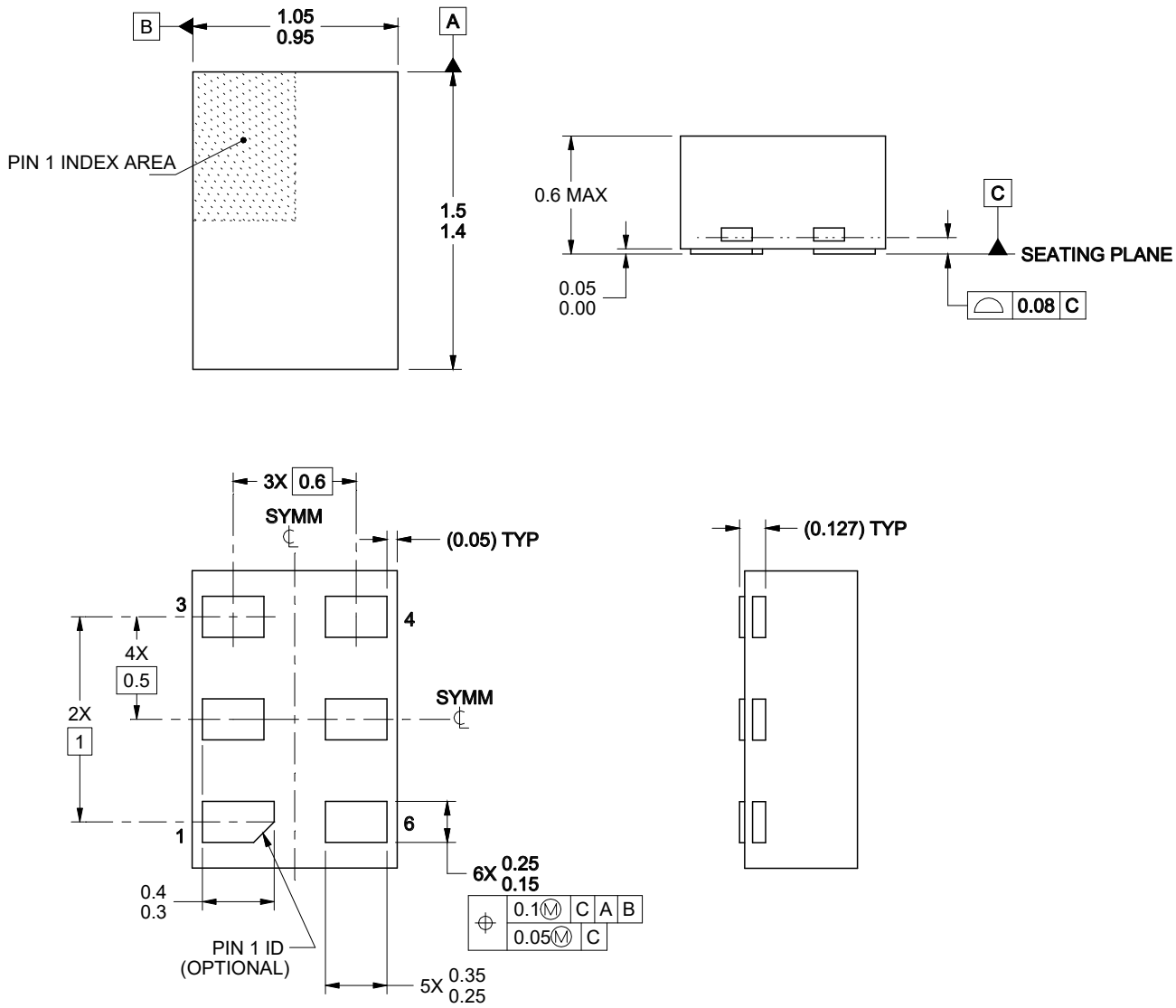
17.1 SC70-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	e1	L	θ
Min	0.90	0.00	0.90	0.15	0.08	1.80	1.15	2.15	0.65	1.20	0.26	7°
Max	1.10	0.10	1.00	0.35	0.15	2.25	1.35	2.45	TYP	1.40	0.46	REF.

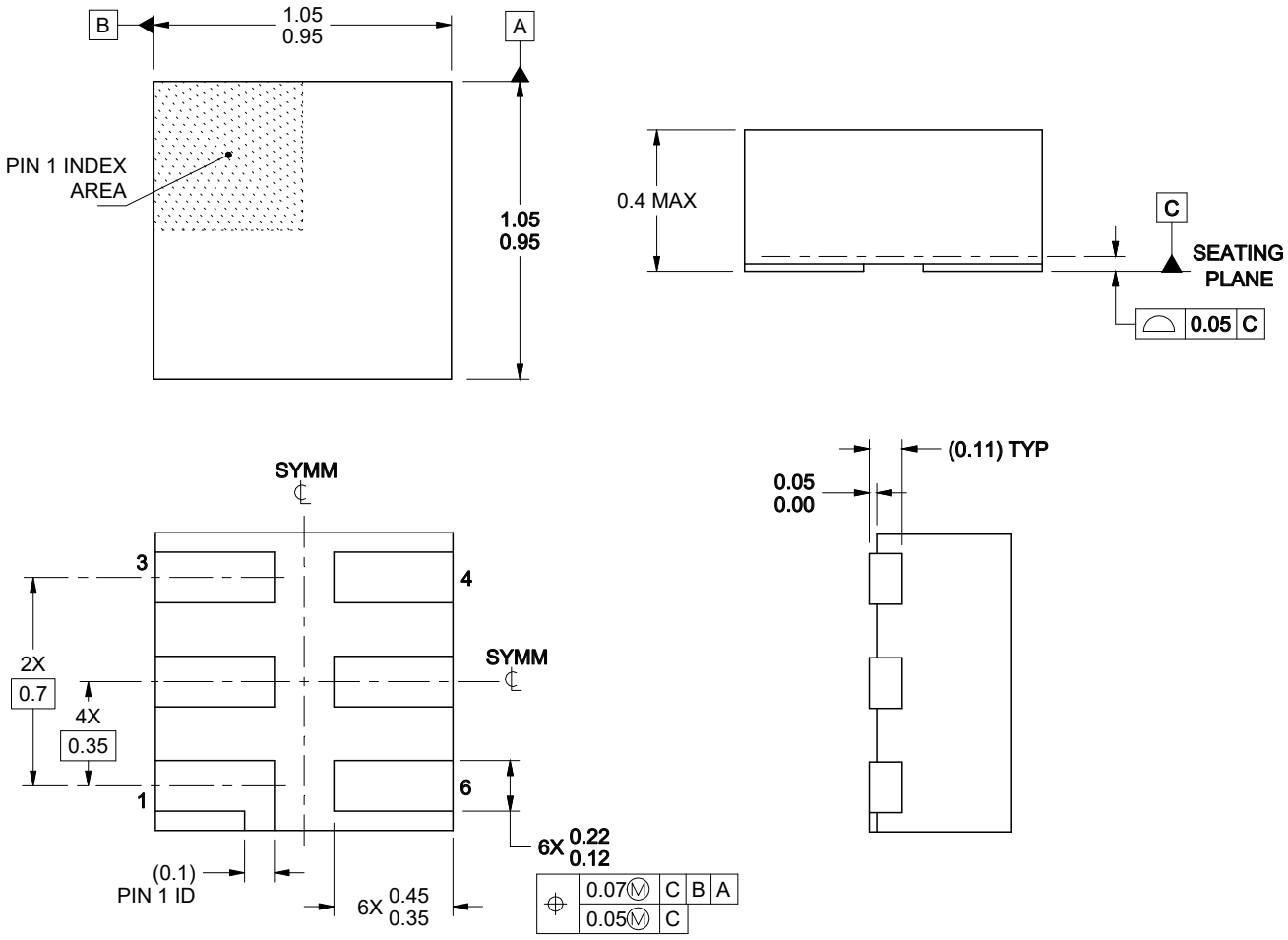
17.2 DRY (USON-6) Package Outline Dimensions



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

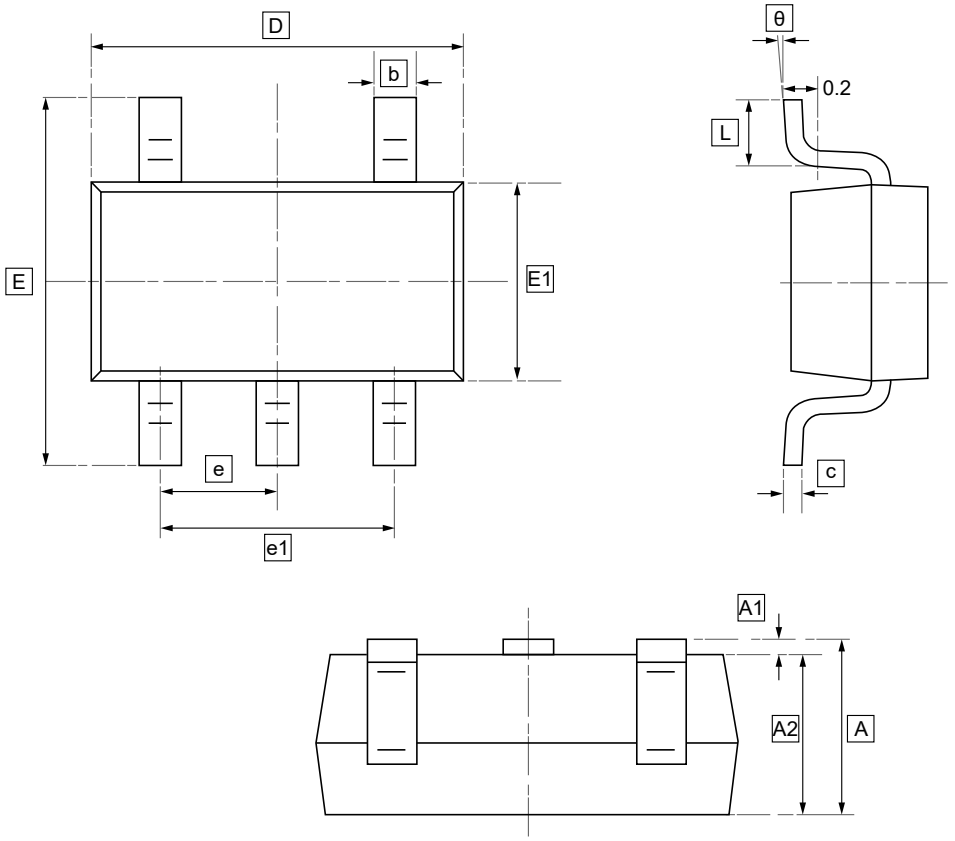
17.3 DSF (X2SON-6) Package Outline Dimensions



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

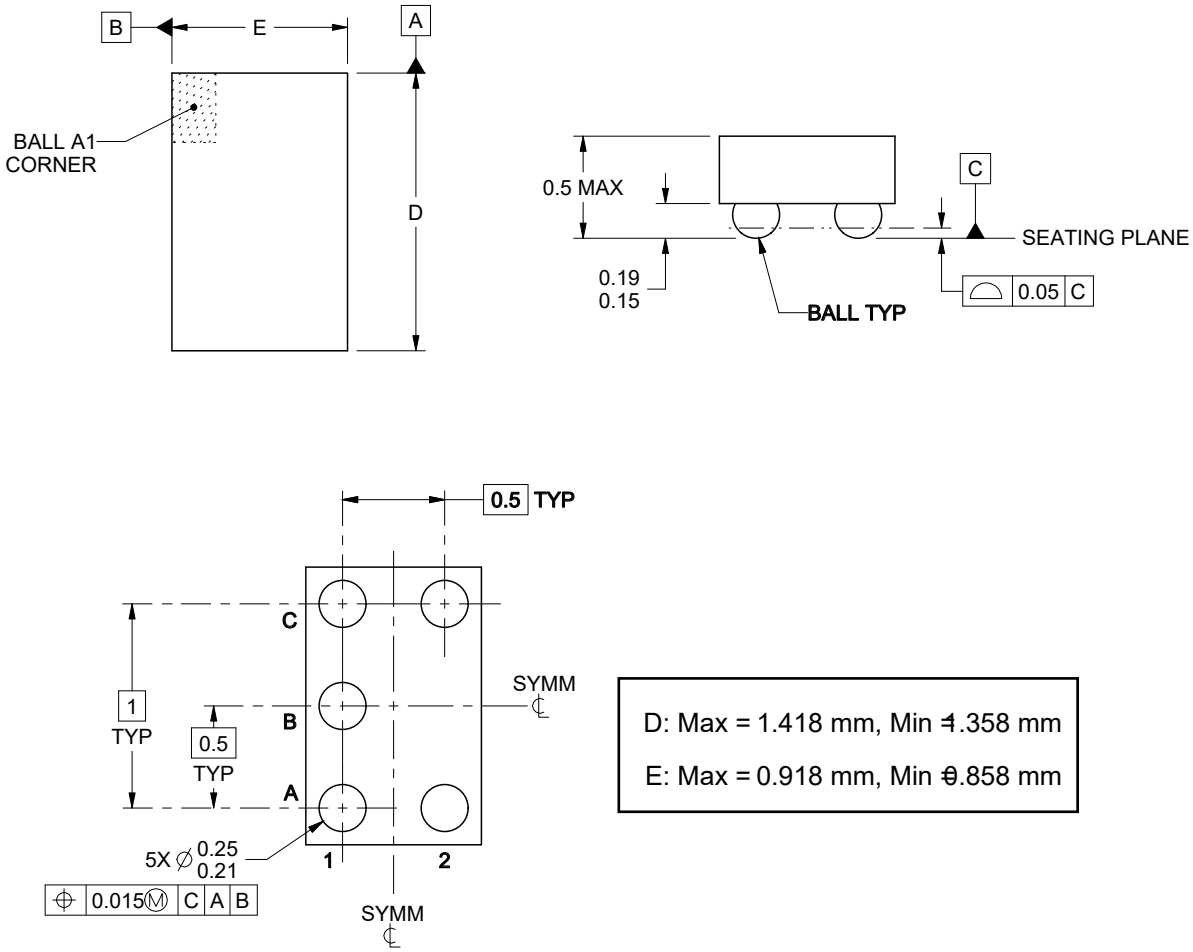
17.4 SOT-23-5 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E1	E	e	e1	L	θ
Min	1.050	0.000	1.050	0.300	0.100	2.820	1.500	2.650	0.950	1.800	0.300	0°
Max	1.250	0.100	1.150	0.500	0.200	3.020	1.700	2.950	BSC	2.000	0.600	8°

17.5 YZP (DSBGA-5) Package Outline Dimensions



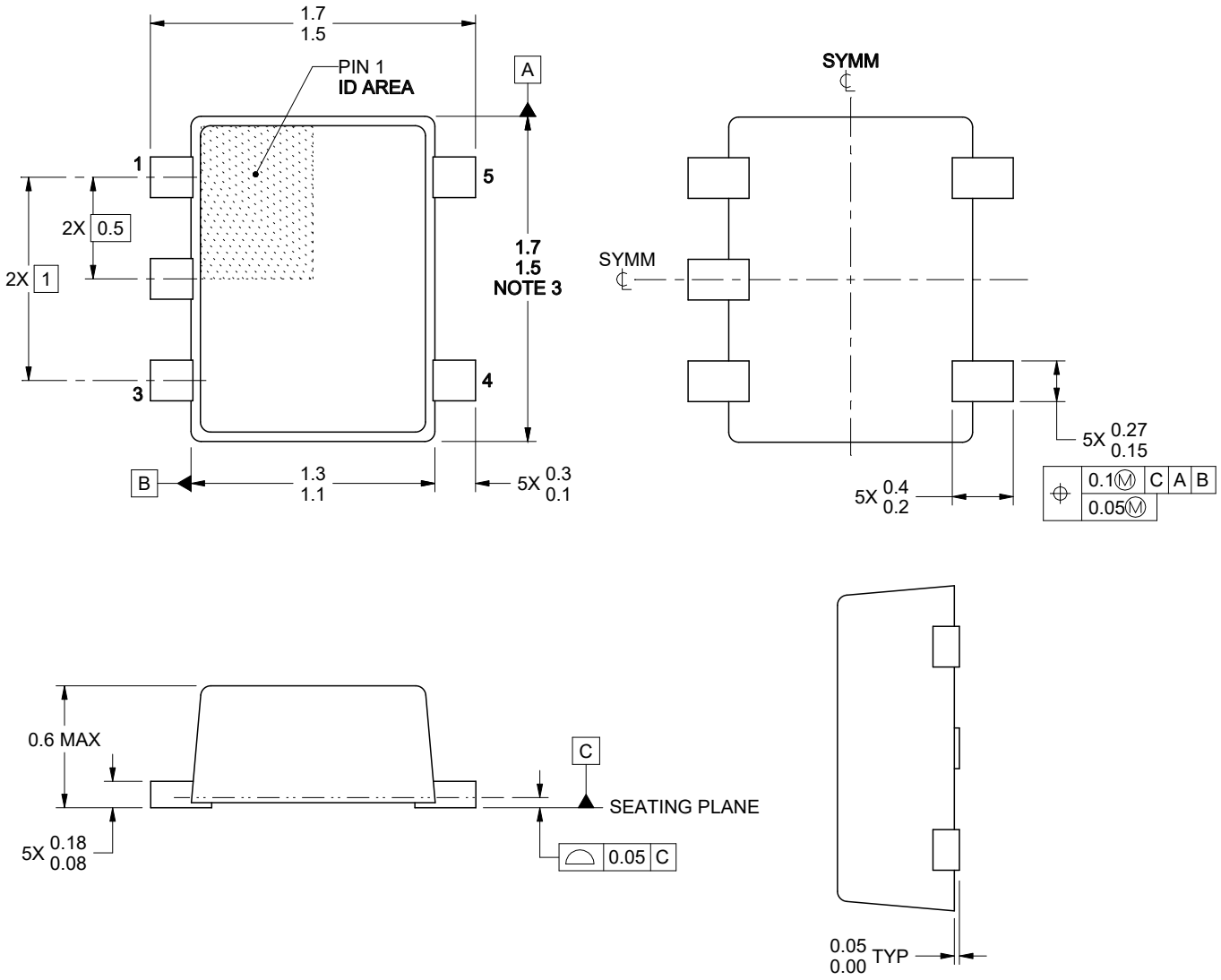
D: Max = 1.418 mm, Min 1.358 mm

E: Max = 0.918 mm, Min 0.858 mm

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

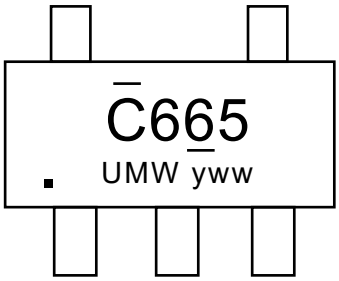
17.6 DRL (SOT-553) Package Outline Dimensions



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

18.Ordering Information



yww: Batch Code

Order Code	Marking	Package	Base QTY	Delivery Mode
UMW SN74LVC1G66DBVR	C665	SOT23-5	3000	Tape and reel
UMW SN74LVC1G66DCKR	C65	SC70-5	3000	Tape and reel
UMW SN74LVC1G66DRLR	C6R	SOT-553	3000	Tape and reel
UMW SN74LVC1G66DRYR	C6	USON-6	3000	Tape and reel
UMW SN74LVC1G66DSFR	C6	X2SON-6	3000	Tape and reel
UMW SN74LVC1G66YZPR	C6N	DSBGA-5	3000	Tape and reel

19.Disclaimer

UMW reserves the right to make changes to all products, specifications. Customers should obtain the latest version of product documentation and verify the completeness and currency of the information before placing an order.

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