1.Description

The UMW IRS2181STR is a high voltage, high speed power MOSFET drivers with dependent high and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET in the high-side configuration which operates up to 700V.

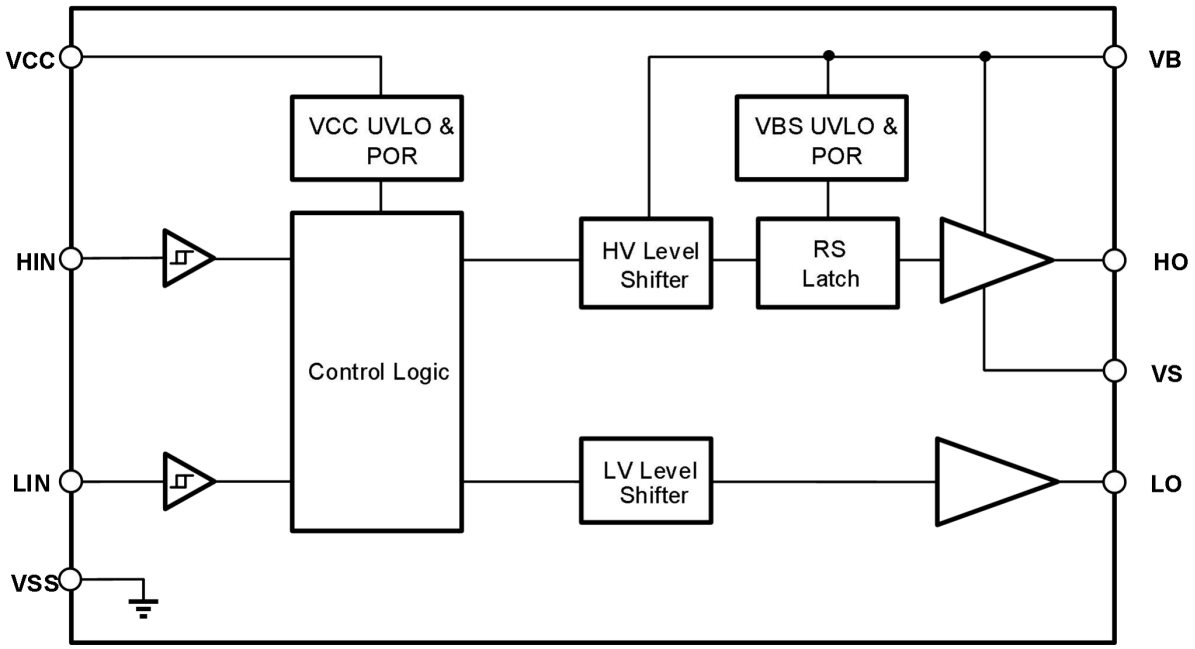
2.Applications

- Motor Control
- Air Conditioners/ Washing Machines
- General Purpose Inverters
- Micro/Mini Inverter Drives

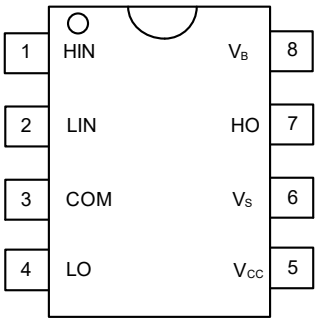
3.Features

- Floating channel designed for bootstrap operation
- Fully operational to +700 V
- 3.3V, 5V and 15V input logic compatible
- dV/dt noise Immunity ±50 V/nsec
- Allowable negative Vs capability: -9V
- Gate drive supply range from 10V to 20V
- Typically output Source/Sink current capability: 4A/4A
- Undervoltage lockout for both channels
  --UVLO forward 8.9V
  --UVLO reverse 8.2V
- Turn-on/Turn-off propagation delay -
  - Ton/Toff =130ns/130ns
- Matched propagation delay for both channels

4.Functional Block Diagram



5.Pinning Information



SOP-8

Lead Definitions

Number	Symbol	Description
1	HIN	Logic input for high side gate driver output (HO), in phase
2	LIN	Logic input for low side gate driver output (LO), in phase
3	COM	Low side return
4	LO	Low side gate drive output
5	V_{CC}	Low side and logic fixed supply
6	V_S	High side floating supply return
7	HO	High side gate drive output
8	V_B	High side floating supply

6.Absolute Maximum Ratings

Exceeding the limit maximum rating may cause permanent damage to the device. All voltage parameters are rated with reference to V_{SS} and an ambient temperature of 25°C.

Parameter	Symbol	Min	Max	Units
High side floating supply	V_B	-0.3	725	V
High side floating supply return	V_S	V_B-25	V_B+0.3	V
High side gate drive output	V_{HO}	V_S-0.3	V_B+0.3	V
Low side and main power supply	V_{CC}	-0.3	25	V
Low side gate drive output	V_{LO}	-0.3	V_{CC}+0.3	V
Logic input of HIN & LIN	V_{IN}	-0.3	V_{CC}+0.3	V
HBM Model	ESD	1.5		kV
Machine Mode		500		V
IPackage Power Dissipation @ T_A ≤25°C	P_D		0.625	W
Thermal Resistance, Junction to Ambient	Rth_{JA}		200	°C/W
Junction Temperature	T_J		150	°C
Storage Temperature	T_S	-55	150	°C
Lead Temperature (Soldering, 10 seconds)	T_L		300	°C

7.Recommended Operating Conditions

For proper operation, the device should be used under the following recommended conditions. The bias ratings of VS and VSS are measured at a supply voltage of 15V, and unless otherwise specified, the ratings of all voltage parameters are referenced to VSS and the ambient temperature is 25°C.

Parameter	Symbol	Min	Max	Units
High side floating supply	V_B	V_S + 10	V_S + 20	V
High side floating supply return	V_S	-9	700	V
High side gate drive output	V_{HO}	V_S	V_B	V
Low side and main power supply	V_{CC}	10	20	V
Low side gate drive output	V_{LO}	0	V_{CC}	V
Logic input of HIN & LIN	V_{IN}	0	V_{CC}	V
Ambient temperature	T_A	-40	125	°C

8.Electrical Characteristics

Valid for temperature range at T_A=25°C, V_{CC}=V_B=15V, C_L=1nF, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Turn-on propagation delay	t_{ON}	V_S=0V		130	250	ns
Turn-off propagation delay	t_{OFF}	V_S=0V or 700V		130	250	ns
Turn-on rise time	t_R	V_S=0V		15	20	ns
Turn-off fall time	t_F	V_S=0V		10	15	ns
Matched propagation time delay	MT				50	ns
V_{CC} supply UVLO threshold	V_{CCUV+}		8	8.9	9.8	V
	V_{CCUV-}		7.4	8.2	9	V
Hysteresis of V_{CC} UVLO	$V_{CCUVHYS}$			0.7		V
V_{BS} supply UVLO threshold	V_{BSUV+}		8	8.9	9.8	V
	V_{BSUV-}		7.4	8.2	9	V
hysteresis of V_{BS} UVLO	$V_{BSUVHYS}$			0.7		V
High-side floating supply leakage current	I_{LK}	V_B=V_S=700V			50	μA
Quiescent V_B supply current	I_{QBS}	V_{IN}=0V or 5V		50	100	μA
Quiescent V_{CC} supply current	I_{QCC}	V_{IN}=0V or 5V		150	240	μA
Logic “1"input voltage	V_{IH}	V_{CC}=10V to 20V	2.5			V
Logic “0” input voltage	V_{IL}	V_{CC}=10V to 20V			0.8	V
High level output voltage, V_{BIAS} -V_O	V_{OH}	I_O=0A			1.4	V
Low level output voltage, V_O	V_{OL}	I_O=20mA			0.1	V
Logic “1” input bias current	I_{IN+}	LIN=5V		25	60	μA
Logic “0”input bias current	I_{IN-}	LIN=0V			2	μA
Output high short circuit pulsed current	I_{O+}	V_O=0V, PW≤10us	3	4		A
Output low short circuit pulsed current	I_{O-}	V_O=15V, PW≤10us	3	4		A

9.Function Description

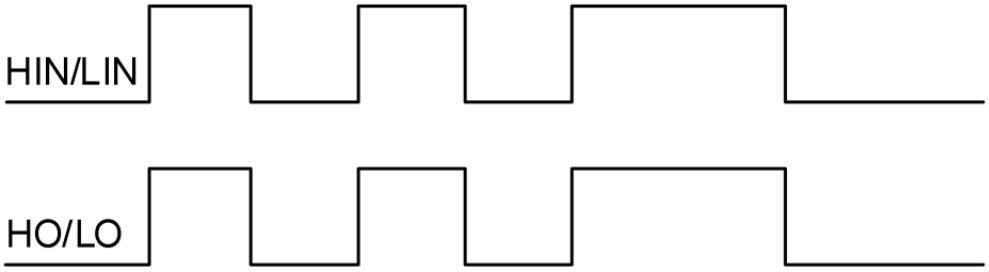


Figure 1. UMW IRS2181STR Input and output timing waveform

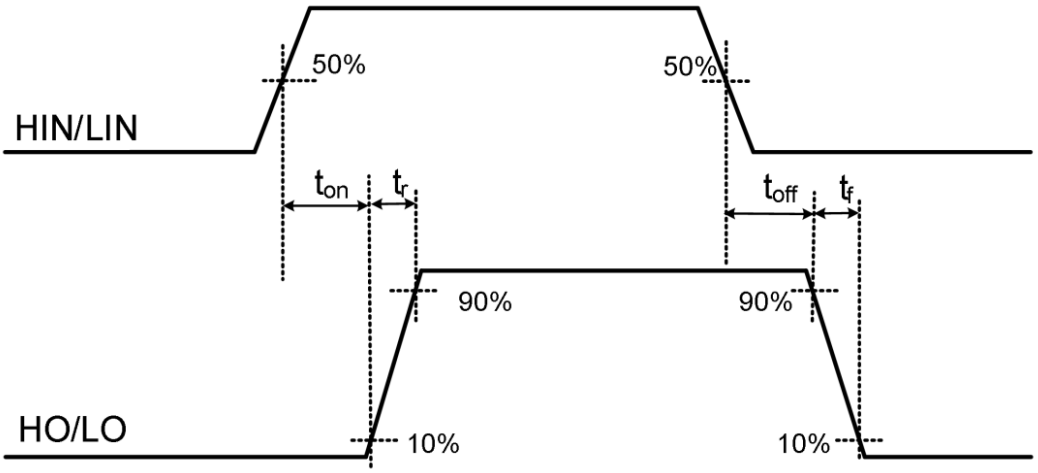


Figure 2. Propagation Time Waveform Definition

10.Function Block Diagram

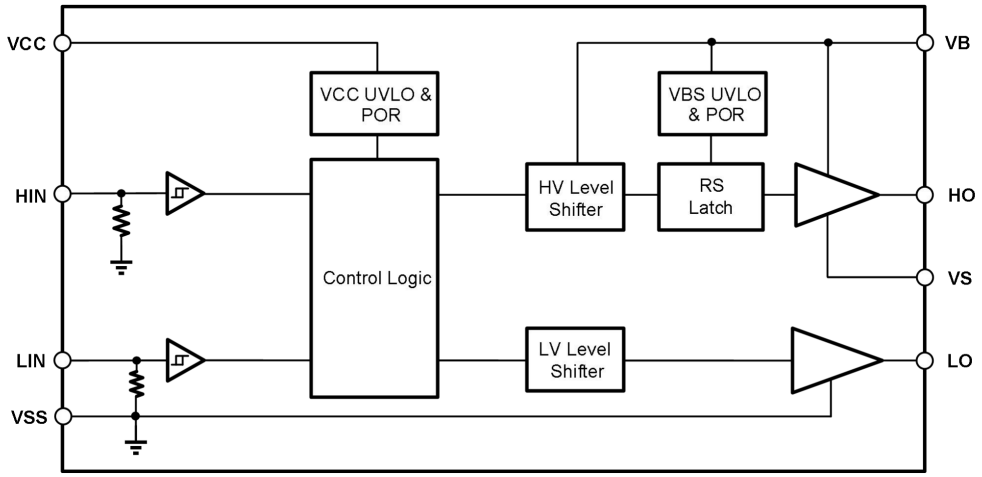


Figure 3. Function Block Diagram of UMW IRS2181STR

11.Application Message

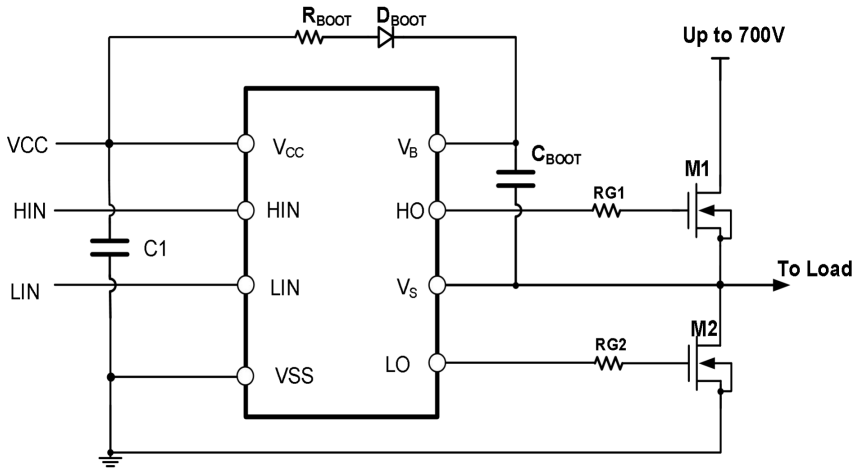
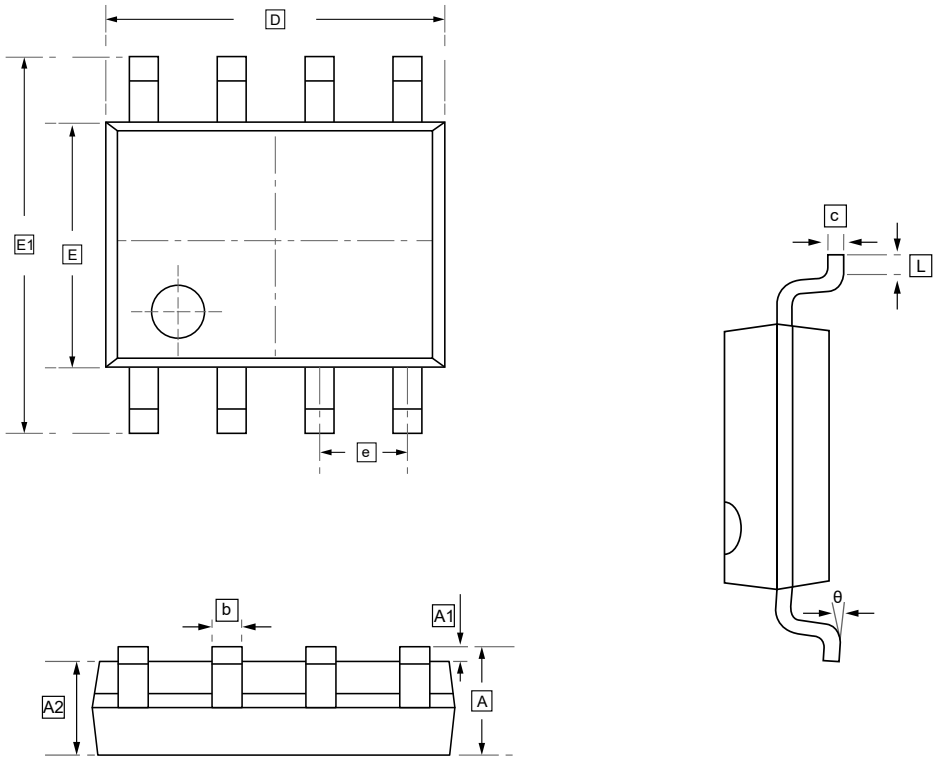


Figure 4. Typical application circuit of UMW IRS2181STR

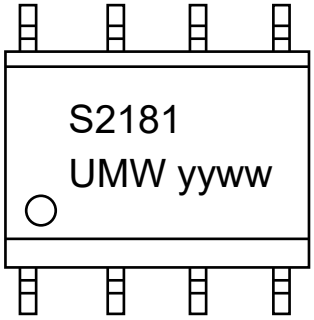
12.SOP-8 Package Outline Dimensions



DIMENSIONS (mm are the original dimensions)

Symbol	A	A1	A2	b	c	D	E	E1	e	L	θ
Min	1.350	0.000	1.350	0.330	0.170	4.700	3.800	5.800	1.270	0.400	0°
Max	1.750	0.100	1.550	0.510	0.250	5.100	4.000	6.200	BSC	1.270	8°

13.Ordering information



yy: Year Code
ww: Week Code

Order Code	Package	Base QTY	Delivery Mode
UMW IRS2181STR	SOP-8	2500	Tape and reel

14.Disclaimer

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